Analysis of Ramp Signal Noise in a CMOS Image Sensor with a Column-wise CDS/Single-slope ADC Circuit Array

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ABSTRACT

It is well known fact that the noise in the ramp signal in the CIS (CMOS Image Sensor) with the column-wise CDS (Correlated Double Sampling)/ADC (Analog-to-Digital Converter) circuit emerges into horizontal line (row-wise) noise on the output image. This noise is one of the most critical performance limits in the CIS with the column-wise CDS/ADC circuit. According to analysis of the single-slope ADC with the CDS circuit, the amount of noise on the output image highly depends on the frequency component of the ramp signal noise. Furthermore, the noise frequency that has the maximum effect on the output image is dependent on the incident light intensity. Analysis and experimental result shows that noise within 10 kHz to 100 kHz range is the most critical component and it overlaps the fundamental frequency of the ramp signal. Therefore, it cannot be removed by filtering. Then, various sources of the ramp signal noise which causes horizontal line noise on the output image have been analyzed. Regarding the CIS operation, there are three major sources. The first is intrinsic noise occurring in a ramp generator. The second is power line noise caused by the switching and the voltage drop in the CDS circuit block and the last one is substrate noise from digital circuits. The amount of noise contribution from each noise source has been measured through experiment. Measured code variation of CDS output by intrinsic noise is 0.20 code, code variation by power line noise is 0.25 code, and code variation by substrate noise is 1.81 code. These measurement results show that the substrate noise is the major source of the ramp signal noise among them. Therefore, to reduce the ramp signal noise which causes H-line noise, not only a well-designed ramp generator with low noise should be considered from the early phase of design, but the substrate noise in the ramp generator should be suppressed by various circuit design techniques.

Key words: CMOS image sensor; ramp signal noise; column-wise CDS/ADC; single-slope ADC; correlated double sampling; horizontal-line noise; ramp generator; substrate noise;

INTRODUCTION

Image sensor types can broadly be classified into a CCD (Charge-Coupled Device) and a CIS (CMOS Image Sensor). Since recently developed CISs are fabricated using standard CMOS process with no or minor modification, a CIS overcomes many shortcomings of the CCD, e.g., readout can now be very fast, and it consumes very low power and uses low operation voltage, while random access enables selective readout of regions-of-interest [1]. Also, due to using standard process, CISs spend

Fig. 1: Block diagram of CIS with column-wise CDS/ADC circuit

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lower cost and can be integrated with various CMOS circuits for image signal processing. Therefore, a CIS currently becomes the more dominant technology for image sensors.

A CIS can be generally classified into three types according to the A/D conversion method. The first is the chip level approach [2][3]. A single conventional ADC (Analog-to-Digital Converter) serves the entire image sensor. Since there is only a single ADC, it must be of very high speed (proportional to the number of pixels in the image sensor). The second approach is to use a pixel level ADC [4][5]. A pixel level ADC means that every pixel has an ADC and all ADCs operate at the same time. The previous works show that pixel level A/D conversion should achieve the highest SNR (Signal-to-Noise Ratio) and the lower power consumption, since it is performed in parallel, close to where the signals are generated, and can be operated at very low speed [6][7]. However, to implement this ADC approach, a very larger pixel space is occupied and the memories to store digital bits of each pixel are needed. Finally, the third is the column level (column-wise ADC) approach. The array of ADCs is placed at the bottom of the sensor array and each ADC is dedicated to one or more columns of the sensor array. The ADCs are operated in parallel and, therefore, the low-to-medium speed (proportional to the number of rows in the image sensor) ADC architecture can be employed. Since this approach has the advantages such as low operating frequency, low power consumption, small circuit size and good offset cancellation capability, it is widely used in the current CISs.

The column-wise ADC architecture, researched until now, can be grouped into a successive approximation ADC [8][9], an algorithmic ADC [10][14], a ΣΔ ADC [11] and a single-slope ADC [12]-[14].

Generally, due to the mismatch every column, there is column-wise FPN (Fixed Pattern Noise) on the output image of the CIS with the column-wise ADC. Also, especially in the CIS employing a single-slope ADC, row-wise noise called H-line (Horizontal-line) noise occurs. This noise has more critical effect on the output image quality. This noise is mainly caused by the noise injected into the output of the ramp generator used as the reference signal of A/D conversion.

Therefore, in this paper, the experimental result that temporal H-line noise on the output image is caused by the ramp signal noise used in the column-wise CDS (Correlated Double Sampling)/ADC circuit is shown. Also, various sources of the ramp signal noise causing this noise phenomenon are analyzed and the amount of noise contribution from each noise source through experiments is provided.

The rest of the paper is organized as follows. Next, the operation principle of the CIS with the column-wise CDS/ADC circuit is described. Section 3 discusses the effect of the ramp signal noise on the output image with H-line noise and the sources of the ramp signal noise in the CIS. Section 4 is devoted to the experimental results. Finally, conclusions are provided in Section 5.

**Operation Principle Of Cis With Column-Wise Cds/Adc Circuit:**

In this section, the operation principle of the CIS with the column-wise CDS/ADC circuit are presented. Fig. 1 shows the block diagram of the CIS. The APS (Active Pixel Sensor) array converts the incident photons into the pixel voltage signal. The column-wise readout circuitry consists of the CDS circuit array and the n-bit register array proportional to the number of columns, a ramp generator and an n-bit digital counter. Flicker noise and pixel FPN are reduced from the pixel voltage signal by the CDS circuit. Then, its voltage signal is converted into digital bits with reference to the output of a ramp generator and they are stored in the register. The output of a ramp generator is connected to the input nodes of all CDS circuits. It can be obtained by using the continuous output of an integrator which consists of an OTA (Operational Transconductance Amplifier), a resistor, a capacitor, and a switch and the discrete output of a DAC (Digital-to-Analog Converter) which has the output of a digital counter as its input.

![Fig. 2: Schematic of 4-TR APS](image-url)
Operation Principle of APS and Column-wise CDS/ADC Circuit:

APSs employ a photodiode (PD\(_{(i,j)}\)) and a pixel readout circuit of four transistors in a pixel P\((i,j)\): a photodiode reset gate (M\(_{RG,(i,j)}\)), a transfer gate (M\(_{TG,(i,j)}\)), a row select gate (M\(_{SEL,(i,j)}\)) and a source follower gate (M\(_{SF,(i,j)}\)). The schematic of this pixel is shown in Fig. 2. Incident photons are converted to charges which are accumulated by the PD\(_{(i,j)}\) during an integration time. The M\(_{TG,(i,j)}\) transfers the accumulated charge on the photodiode to the floating node (D\(_{(i,j)}\)) and can also be kept at a constant intermediate voltage throughout to avoid blooming and to reduce switching noise. The charge-to-voltage conversion occurs at the node D\(_{(i,j)}\) capacitance, which comprises the parasitic capacitances of M\(_{RG,(i,j)}\), M\(_{TG,(i,j)}\) and M\(_{SF,(i,j)}\) connected to that node. At this time, the M\(_{SF,(i,j)}\) acts as a buffer amplifier to isolate the sensing node; the load of this buffer (the active current-sink load, M\(_{LOAD,(j)}\)) is located on each column rather than on each pixel to keep the fill factor high and to reduce pixel-to-pixel variations.

The M\(_{RG,(i,j)}\) controls an integration time and is usually implemented with an NMOS transistor. Since no additional well is required for NMOS implementation, this allows a higher fill factor. However, an NMOS transistor with the power supply voltage (V\(_{DD}\)) on both gate and drain can only reach the node D\(_{(i,j)}\) voltage of V\(_{D(i,j),RST}\), thereby decreasing the DR (Dynamic Range) of the pixel. Here, the pixel reset voltage (V\(_{D(i,j),RST}\)) can be expressed as

\[
V_{D(i,j),RST} = V_{DD} - V_{MSF,(i,j),th}
\]

where V\(_{MRG,(i,j),th}\) is the threshold voltage of the M\(_{RG,(i,j)}\). The M\(_{SEL,(i,j)}\) acts as the switch selecting all pixels in the same row.

![Fig. 3: Schematic of column-wise CDS/ADC circuit](image)

Also, as shown in Fig. 3, each column-wise readout circuit is composed of 4 switches, 3 capacitors, 4 inverters which are operated as a comparator, and an n-bit register storing digital bits corresponding to the analog pixel signal value from n-bit counter.

The operation principle of the APS with four transistors using pinned photodiode [15]-[17] and the column-wise CDS/ADC circuit is described here with reference to Fig. 2, Fig. 3 and Fig. 4, which illustrate the schematic of them and the timing diagram of their operation. Generally, the operation can be divided into five main phases: pixel reset, CDS reset, pixel read, CDS read and ADC.

(a) The pixel reset phase. First of all, by turning on the M\(_{SEL,(i,j)}\), all pixels in the same row are simultaneously selected. Later, to eliminate charges accumulated by thermal and flicker noise in the node D\(_{(i,j)}\), the capacitance of the D\(_{(i,j)}\) node is charged to V\(_{D(i,j),RST}\) by turning on the M\(_{RG,(i,j)}\). At this time, the V\(_{PIXEL(i,j),RST}\) can be expressed as Eq. (2) because of the threshold voltage (V\(_{MSF,(i,j),th}\)) drop of the M\(_{SF,(i,j)}\).

\[
V_{PIXEL(i,j),RST} = V_{D(i,j),RST} = V_{M_{SF,(i,j),th}}
\]

(b) The CDS reset phase. After the pixel reset phase, the CDS reset phase starts. V\(_{1}\) becomes V\(_{PIXEL(i,j),RST}\) because S\(_{1}\) is on, and V\(_{IN}\) becomes the switching threshold voltage (V\(_{INV1,th}\)) of the INV\(_{1}\), because the switch S\(_{2}\) is on, and then the input voltage of the INV\(_{1}\) is identical with the output voltage. That is,
After the CDS reset phase, the voltage ($V_{C1}$) of the capacitor $C_1$ is given by

$$V_{C1} = V_{\text{PIXEL(RST)}} - V_{\text{IN,RST}}$$

$$= V_{DD} - V_{M_{\text{ext},1,th}} - V_{M_{\text{ext},1,th}} - V_{\text{IN,th}}$$

(c) The pixel read phase. Firstly, the capacitor ($C_{PD(i,j)}$) of the PD$(i,j)$ is discharged through a constant integration time ($T_{\text{INT}}$) by the photocurrent ($I_{PD(i,j)}$) proportional to the incident illumination. The quantity of positive charges discharged in the $C_{PD(i,j)}$, which corresponds to the pixel signal value induced by the incident light, can be expressed as Eq. (5).

$$Q_{PD(i,j),\text{SIG}} = I_{PD(i,j)} \times T_{\text{INT}}$$

After the integration phase, the $M_{\text{TG(i,j)}}$ is turned on to transfer the $Q_{PD(i,j),\text{SIG}}$ to the $D(i,j)$ node. Then, at the end of this time, the $D(i,j)$ node voltage ($V_{D(i,j),\text{READ}}$) changes as

$$V_{D(i,j),\text{READ}} = V_{D(i,j),\text{RST}} - V_{PD(i,j),\text{SIG}}$$

$$= V_{D(i,j),\text{RST}} - \frac{Q_{PD(i,j),\text{SIG}}}{C_{PD(i,j)}}$$

$$= V_{DD} - V_{M_{\text{ext},1,th}} - \frac{I_{PD(i,j)} \times T_{\text{INT}}}{C_{PD(i,j)}}$$

where $V_{PD(i,j),\text{SIG}}$ is the discharged voltage proportional to $Q_{PD(i,j),\text{SIG}}$ in the $C_{PD(i,j)}$ and means the voltage corresponding to the pixel signal value induced by the incident light. Also, similar to the pixel reset phase, the $V_{\text{PIXEL(i,j)}}$ at the read step can be expressed as Eq. (7).

$$V_{\text{PIXEL(i,j),READ}} = V_{D(i,j),\text{READ}} - V_{M_{\text{ext},1,th}}$$

$$= V_{DD} - V_{M_{\text{ext},1,th}} - \frac{I_{PD(i,j)} \times T_{\text{INT}}}{C_{PD(i,j)}} - V_{M_{\text{ext},1,th}}$$

(d) The CDS read phase. After the pixel read phase, the terminals of the $C_1$ are floating nodes and the $V_{C1}$ remains as Eq. (4). Then, the CDS read phase begins. When $S_1$ is on, $V_1$ becomes $V_{\text{PIXEL(i,j),READ}}$, and after $S_1$ is off, $V_{IN}$ becomes

$$V_{\text{IN,READ}} = V_{\text{PIXEL(i,j),READ}} - V_{C1}$$

From Eq. (4) and (7), Eq. (8) yields

$$V_{\text{IN,READ}} = V_{\text{IN,th}} - V_{PD(i,j),\text{SIG}}$$

$$= V_{\text{IN,th}} - \frac{I_{PD(i,j)} \times T_{\text{INT}}}{C_{PD(i,j)}}$$

In Eq. (9), the threshold voltages of the gate $M_{\text{RG(i,j)}}$ and $M_{\text{SF(i,j)}}$ are canceled out, so the pixel FPN is reduced. Here, since the input voltage of the $\text{INV}_1$ is $V_{\text{IN,READ}}$ meaning logical low state, the output state of the $\text{INV}_1$ becomes logical high state. Therefore, the final CDS output ($V_{\text{CDS(i,j),OUT}}$) state becomes logical low state by three inverter chain.

(e) The ADC phase. After the CDS read phase, the $n$-bit counter starts and the ramp signal ($V_{\text{RAMP,OUT}}$) concurrently ramps upward from the offset voltage ($V_{\text{RAMP,OFFSET}}$) of the ramp signal. At this time, $V_1$ and $V_{\text{IN}}$ in the floating state simultaneously increase with $V_{\text{RAMP,OUT}}$. When $V_{\text{IN}}$ exceeds $V_{\text{IN,th}}$, the output state of the $\text{INV}_1$ becomes logical low state. Therefore, the $V_{\text{CDS(i,j),OUT}}$ state changes from logical low state to logical high state. Here, the transition of $V_{\text{CDS(i,j),OUT}}$ is used to enable a register to latch digital bits corresponding to $V_{PD(i,j),\text{SIG}}$ from a $n$-bit counter. Therefore, A/D conversion is complete.

These (a) The reset phase and (c) The read phase are repeated every row, and then before A/D conversion, low frequency noise (e.g. flicker noise) and FPN such as offset and mismatch occurring in the APS are reduced through the CDS operation to obtain more noiseless images. Also, through (b) The CDS reset phase, (d) The CDS read phase, and (e) The ADC phase, the readout operation is performed and the analog pixel signal value is converted into the digital bits. These are used to perform the post image processing using an ISP (Image Signal Processor), and then the processed results is displayed on the monitor.

Analysis of Effect of Ramp Signal Noise on Output Images And Ramp Signal Noise Sources:

The output SNR of the single-slope ADC used in the column-wise readout circuit is highly dependent on the spectral purity of the ramp signal because, during A/D conversion, the correlated-double-sampled analog data is compared with the ramp signal.

In the case of the CIS with a single-slope ADC, noise in the ramp signal may cause temporal noise on the output image. Because outputs of the pixel array
in the same row are simultaneously encoded into digital code, the pixels in the same row experience the same noise in the ramp signal during the readout operation. This causes the output image of the CIS to have noisy and flickering line (H-line noise phenomenon) in the row-wise direction as shown in Fig. 5. To overcome the problem arisen from noise in the ramp signal, the detailed information about transfer function from the ramp noise to the noise on the output image should be prior analyzed. Therefore, in this section, the relationship between the ramp signal noise and its effect on the output image is investigated and various sources of the ramp signal noise which causes H-line noise are analyzed and the amount of noise contribution from each noise source through the simulation is provided.

3.1. Analysis of Effect of Ramp Signal Noise

The simplified schematic of the column-wise CDS circuit and the APS mentioned in Section 2 is shown in Fig. 6. Every column in the CIS chip is equipped with a readout circuit with a CDS/ADC circuit. Here, to verify the effect of the ramp signal noise, the operation principle of the CDS/ADC circuit considering the noisy ramp signal $V_{RAMP,OUT}$ unlike the noiseless ramp signal of Section 2 is described as the following two steps.

(a) At the first step, the CDS circuit samples the pixel signal value ($V_{PIXEL(i,j),READ}$) in the pixel read phase, and the pixel reset value ($V_{PIXEL(i,j),RST}$) in the pixel reset phase into corresponding capacitors, the $C_2$ and $C_1$, respectively as described in Section 2. At the moment $V_{PIXEL(i,j),READ}$ is sampled into the $C_2$, dc offset value of the ramp signal ($V_{RAMP,OFFSET}$) is also sampled as a reference voltage level of $V_{C2}$. If there is noise in the $V_{RAMP,OFFSET}$, the noise will be also sampled into the $C_2$. In the mathematical form, the voltage stored in the $C_2$ and $C_1$ after the first step can be expressed as follow.

$$V_{C_2}=V_{PIXEL(i,j),READ}+ (V_{RAMP,OFFSET}+ V_{RAMP,NOISE}(t))$$ (10)

$$V_{C_1}=V_{PIXEL(i,j),RST}+ V_{INV1,th}$$ (11)

In Eq. (10) and (11), all signals except for $V_{RAMP,NOISE}(t)$ are assumed to be noiseless. The time of the moment when $V_{C2}$ is sampled is denoted as $t_1$, and the noise in the ramp signal at time $t_1$ is expressed as $V_{RAMP,NOISE}(t_1)$.

(b) At the second step, ($V_{C2}-V_{C1}$) is pulled up by the ramp signal and compared with $V_{INV1,th}$. The voltage applied at the inverter input node is

$$V_{IN}=V_{C_2}-V_{C_1}+ V_{RAMP,RAMPING} + V_{RAMP,NOISE}(t_2)$$ (12)

where $V_{RAMP,RAMPING}$ denotes the ramp signal except for its dc offset voltage ($V_{RAMP,OFFSET}$) and $t_2$ denotes time of the moment when $V_{IN}$ becomes greater than $V_{INV1,th}$. From Eq. (1), (5), (10) and (11), Eq. (12) yields the following result.

$$V_{IN}=V_{RAMP,RAMPING}+ V_{INV1,th} + V_{PD(i,j),SIG}(t_2)$$

$$+ V_{RAMP,NOISE}(t_3)- V_{RAMP,NOISE}(t_1)$$ (13)

In Eq. (13), $V_{PD(i,j),SIG}$ represents the only meaningful APS output induced by the light, and $V_{IN}$ makes the transition from logical low state to logical high state when $V_{RAMP,RAMPING}$ is greater than $V_{PD(i,j),SIG}$.

According to Eq. (13), the only difference of noise amount between at the time $t_2$ and $t_1$ has an effect on the decision of $INV_1$. If we assume that noise in the ramp signal is the single tone sine wave, then the effect of the ramp noise may emerge into noise (or flicker) on the output image with different amount according to phase difference of the sine wave noise. If the wavelength of noise is much...
longer than \((t_2-t_1)\), noise has no effect on the output image because the code variation of the CDS circuit output is very small. To make the amount of the effect of the sine wave noise maximum, the period of the sine wave noise should be \(2\times(t_2-t_1)\). On the contrary, if the period of the sine wave noise corresponds with \((t_2-t_1)\), the sine wave is canceled out because of its periodicity at time \(t_1\) and \(t_2\).

In general, the sine wave noise whose frequency is
\[
f_{\text{NOISE,MAX}} = \frac{1}{2(t_2-t_1)} N, \quad N=1,3,5,\ldots,2n+1,\ldots
\]
has a maximum effect on the output image. If the frequency is
\[
f_{\text{NOISE,MIN}} = \frac{1}{2(t_2-t_1)} N, \quad N=2,4,6,\ldots,2n,\ldots
\]
then the sine wave noise has a minimal effect on the output image. Fig. 7 illustrates how this noise in the ramp signal affects the output of the CDS circuit. According to equation (14) and (15), however, since \(t_2\) is dependent on the light intensity, the frequency component that has a maximum effect is also dependent on the light intensity.

### 3.2. Analysis of Ramp Signal Noise Sources:

#### 3.2.1. Intrinsic Noise of the Ramp Generator:

There are three main fundamental intrinsic noise mechanisms: thermal, shot, and flicker [18]. All three mechanisms occur in devices such as a resistor, a bipolar transistor, and a MOS transistor.

To estimate the amount of intrinsic noise in the ramp generator which consists of resistors, bipolar transistors, and MOS transistors, the intrinsic noise transient simulation using the ELDO simulator was performed with the ramp generator circuit shown in Fig. 8. Here, intrinsic noise occurs in the R\(_{\text{INT}}\), the BGR (Band-Gap voltage Reference) and DAC, the OTA, and the Buffer. Table 1 presents the amount of intrinsic noise of each block. While the Ideal term

Fig. 7: Illustration of CDS operation and ramp noise

Fig. 8: Structure of ramp generator
means that the components used in the simulation are ideal blocks which do not generate intrinsic noise, the Real term means that they are real components which generate intrinsic noise. The existence of Buffer block generates 3000 μV_{p-p} (Case 4 and Case 5). However, the load capacitor of buffer \( C_L \) decreases intrinsic noise of the ramp output due to lowpass filtering, and the major contributor of intrinsic noise is the Buffer block, because intrinsic noise before the buffer is lowpass-filtered by the integrator. The simulated total variation of the ramp output is about 1000 μV_{p-p} that corresponds to the CDS circuit output error of 0.23 code.

**3.2.2. Power Line Noise due to Switching in the CDS Circuit:**

In the case of the column-wise CDS/ADC circuits, their parallel layout pattern corresponding to the number of columns is required, and every column-wise CDS/ADC circuit shares the power line with the ramp generator. Therefore, their power line has long distance, so voltage drop exists along the power line. Also, the switching of the column-wise CDS/ADC causes the switching noise over the power line. These power noises could affect the output of the ramp generator and generate the output variance of the CDS circuit. To verify these facts, the power line model assuming metal 2 layer (sheet resistance: 0.05 Ω/□, area capacitance: 13 a/μm², fringe capacitance: 25 a/μm²) power line for 320 column-wise CDS/ADC circuits is established according to the layout of the CDS circuit block. From the CDS

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**Table 1:** Simulation results of intrinsic noise of ramp generator

<table>
<thead>
<tr>
<th>Case</th>
<th>\text{BGR\textsuperscript{+} DAC}</th>
<th>\text{Real}</th>
<th>\text{BGR\textsuperscript{-} DAC}</th>
<th>\text{Real}</th>
<th>\text{Buffer}</th>
<th>\text{Real}</th>
<th>\text{Output noise (μV}_{p-p} \right)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ideal</td>
<td>Real</td>
<td>Ideal</td>
<td>Real</td>
<td>0 pF</td>
<td>0 pF</td>
<td>5</td>
</tr>
<tr>
<td>2</td>
<td>Real</td>
<td>Real</td>
<td>Ideal</td>
<td>Real</td>
<td>0 pF</td>
<td>0 pF</td>
<td>1500</td>
</tr>
<tr>
<td>3</td>
<td>Ideal</td>
<td>Real</td>
<td>Ideal</td>
<td>Real</td>
<td>0 pF</td>
<td>0 pF</td>
<td>3000</td>
</tr>
<tr>
<td>4</td>
<td>Real</td>
<td>Real</td>
<td>Real</td>
<td>Real</td>
<td>0 pF</td>
<td>0 pF</td>
<td>4000</td>
</tr>
<tr>
<td>5</td>
<td>Real</td>
<td>Real</td>
<td>Real</td>
<td>Real</td>
<td>10 pF</td>
<td>0 pF</td>
<td>7000</td>
</tr>
<tr>
<td>6</td>
<td>Real</td>
<td>Real</td>
<td>Real</td>
<td>Real</td>
<td>10 pF</td>
<td>10 pF</td>
<td>3000</td>
</tr>
<tr>
<td><strong>Contributed noise (μV}_{p-p}</strong></td>
<td>1395</td>
<td>5</td>
<td>2995</td>
<td>3000</td>
<td>1000</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Fig. 9:** RC modeling of power line for CDS circuit block

**Fig. 10:** RLC modeling of power pad

**Fig. 11:** Simulation result of power line noise for RLC modeling
Fig. 12: Simulated code variation of CDSs by power line noise

![Simulated code variation of CDSs by power line noise](image)

Circuit block layout, the resistance and the parasitic capacitance of the power line can be extracted and the RC modeling for the power line can be done as illustrated in Fig. 9. Also, the power pad can be modeled as shown in Fig. 10 by using the normal value of R, L, and C.

When the switching and the voltage drop of the CDS circuit block occurs, in the case of using these power line and pad model, the simulated power line noise phenomenon is shown as Fig. 11. The peak-to-peak variation of VDD at the 160-th CDS circuit is 1.315 mV.

Fig. 13: Substrate noise coupling in mixed-signal circuit

![Substrate noise coupling in mixed-signal circuit](image)

The CDS circuit output variation by this power line noise is transiently simulated. Fig. 12 shows the simulated CDS code variation along the column number. The maximum code variation by power line noise is about 0.43 code and its mean is 0.28 code.

3.2.2. Power Line Noise due to Switching in the CDS Circuit:

A CIS includes digital circuits such as register arrays, control circuits, and an ISP. These digital circuits generate the substrate noise due to large numbers of switching activities. The substrate noise generated from digital circuits is coupled with analog circuits such as the ramp generator and the CDS/ADC circuit as shown in Fig. 13. The substrate noise coupled with the ramp generator causes the noisy ramp output.

Experimental Results:

4.1. Effect of Ramp Signal Noise:

In this section, the test setup and the experimental result for the effect of the ramp signal noise on output images are provided.

4.1.1. Test Setup:

To measure the effect of the ramp signal noise on the output image, first of all, a full CIS chip which can capture the scenery needs to be fabricated. Fig. 14 shows the block diagram of the implemented full CIS chip. It consists of an APS array, a column-wise readout circuit array, a variety of decoders and drivers, and bias circuits.

Characteristics of the fabricated chip are summarized in Table 2. The APS array adopts 4-transistor structure which has the pixel pitch of 5.6 μm × 5.6 μm and the fill factor of 37 %. Readout circuitry is divided into even column circuit and odd column circuit due to the area limit. There exist a variety of signals which include the ramp signal and the timing control signal out of the chip.
Fig. 14: Block diagram of full CIS chip

Fig. 15: Layout of full CIS chip

Fig. 16: Captured output image of full CIS chip

Fig. 17: Instruments setup for ramp noise test

Fig. 15 shows the layout of the fabricated full CIS chip. Using this chip, the captured output image by a frame grabber is shown in Fig. 16. From Fig. 16, when the ramp signal provided out of the chip is noiseless, there is hardly H-line noise on the output image.

To measure the effect of the ramp signal noise, the implemented full CIS chip with the column-wise CDS/ADC circuit is used as a DUT (Device Under Test). The noise from the noise source is added into the ramp signal as shown in Fig. 17.

4.1.2. Experimental Results:

Fig. 18 shows the output images when the random noise having various magnitudes is added to the ramp signal. It shows that the ramp signal noise generates H-line (i.e. direction in row-wise) noise. Further analysis on the images reveals that the ramp signal noise generates noisy lines only in row-wise direction as depicted in Fig. 19. On the other hand, column-wise noise in Fig. 19 is not influenced by the ramp signal noise because all columns in the same row are processed at the same time and only column-to-column differences can generate such types of noise, i.e. column-wise FPN. This means that the influence of the ramp signal noise on pixel temporal noise is not significant.
Table 2: Characteristics of implemented full CIS chip

<table>
<thead>
<tr>
<th>Process</th>
<th>0.35-μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array format</td>
<td>Total 330-250</td>
</tr>
<tr>
<td></td>
<td>Effective 320-240</td>
</tr>
<tr>
<td>Chip size</td>
<td>3.6 mm × 3.4 mm</td>
</tr>
<tr>
<td>Effective imaging area</td>
<td>1.85 mm × 1.4 mm</td>
</tr>
<tr>
<td>Pixel size</td>
<td>5.6 μm × 5.6 μm</td>
</tr>
<tr>
<td>Fill factor</td>
<td>37 %</td>
</tr>
<tr>
<td>Video output</td>
<td>8/10 bits digital</td>
</tr>
<tr>
<td>Package</td>
<td>48LCC</td>
</tr>
<tr>
<td>Power supply</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>30 mW</td>
</tr>
</tbody>
</table>

Fig. 18: Images of standard resolution chart of various ramp noise amplitudes

Fig. 19: Comparison between column-wise and row-wise noise on image for varying ramp noise amplitude (1 LSB=398.88 μV)

Fig. 20: Output images of various ramp noise frequencies
When the sine wave noise is injected to the ramp signal, output images of the full CIS chip are shown in Fig. 20. It shows that, as the frequency of the noise varies, the amount of the noise on output images also varies. More detailed measurements on the dependency are performed and their results are depicted in Fig. 21. The amount of the noise on output images is quantified by computing standard deviation of all pixel values in a temporally averaged image.

In Fig. 21, three major phenomena are noticed. First, the noise frequency of the maximum effect exists and, in its odd harmonic frequency, local maximums also exist.

Secondly, the less critical effect of the ramp noise appears at the frequency below one kHz and above one MHz. As discussed in Section 3.1, the noise transfer curve below one MHz can be clearly explained by the relationship between the ramp noise frequency and \( (t_2 - t_1) \) time interval. In the case of frequency range above one MHz, the ramp noise is filtered by RC lowpass filter formed by on-resistance of CDS switches and sampling capacitors. The noise below 1 kHz is canceled out by the CDS operation.

Third distinct phenomenon is the maximum frequency dependency on the light intensity of images. Fig. 21 clearly shows the horizontal shift of the graph as the light intensity increases. In Fig. 22, the frequency of maximum noise effect versus the averaged pixel output is depicted.

4.2. Ramp Signal Noise Sources:

In this section, the test setup and the experimental result to verify the sources of the ramp signal noise are provided.

4.2.1. Test Setup:

A test chip has been fabricated with 0.35-μm CMOS process to verify the analysis in Section 3.2. The test chip is composed of 180 column-wise CDS/ADC circuits, a ramp generator consisting of an integrator, a DAC and a BGR, and an on-chip digital noise source as described in Table 3. Fig. 23 shows the layout of this test chip.

The DUT is placed in the shield box to minimize the environmental noise. The variation of the CDS output is measured with an oscilloscope and the noise floor level of the ramp output is measured with a spectrum analyzer and an audio frequency analyzer. The slope of the ramp signal is 1 mV per 83.3 ns (1 code = 83.3 ns).
Table. 3: Digital noise source characteristics

<table>
<thead>
<tr>
<th>Position</th>
<th>On-chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>256 8-bit digital counter</td>
</tr>
<tr>
<td>Number of gates</td>
<td>About 23,000</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>25 MHz</td>
</tr>
<tr>
<td>Power</td>
<td>Separated from analog power</td>
</tr>
<tr>
<td>Distance from readout circuitry</td>
<td>About 500 µm</td>
</tr>
</tbody>
</table>

Fig. 23: Layout of test chip to verify ramp signal noise sources

4.2.2. Experimental Results:

Fig. 24(a) shows the spectrum of the ramp output when only the ramp generator is operating. When the CDS circuits are operating, the noise floor level rose by 5~10 dB as shown in Fig. 4.24(b). When the on-chip digital noise source is operating, harmonics of the digital clock appear as shown in Fig. 4.24(c). In Fig. 4.24, a grid of x-axis expresses 10 MHz and a grid of y-axis expresses 10 dB.

From the result of Section 4.1, whenever the noise having some frequency is injected to the ramp signal, the H-line noise, which has difference of degree, occurs on the output image. However, there is the specific frequency range (10 kHz~100 kHz) to cause more H-line noise according to a time interval of the CDS operation.

From Fig. 24, it is certain that power line noise and substrate noise have an effect on the ramp signal noise. To verify that power line noise and substrate noise have an effect on the formation of the ramp noise of the specific frequency range causing more critical H-line noise, the spectrum of the ramp signal was measured through an audio frequency analyzer as shown in Fig. 25.

Fig. 24: Spectrum of ramp output (until 100 MHz)
Fig. 25: Spectrum of ramp output (until 100 kHz)

As shown in Fig. 25, power line noise and substrate noise have no effect on the formation of the ramp noise of the range of 10 kHz to 100 kHz. Therefore, harmonics of the digital clock from substrate noise largely affects the ramp signal noise generation as shown in Fig. 24(c). This fact can be verified by measuring the code variation of the CDS output by each noise source.

The peak-to-peak variation of the waveform when the ramp generator is not operating is measured as shown in Fig. 26(a). This variation is caused by the noise from the environment and the measurement equipment themselves. The peak-to-peak variation of the ramp signal when only the ramp generator is operating is measured at the ramp generator output node as in Fig. 26(b). The increased variation is caused by intrinsic noise of the ramp generator. The increased variation is about 0.2 mV that can be converted to 0.2 code variation of the CDS output considering the slope of the ramp signal.

Fig. 26: Peak-to-peak variation of ramp generator output

Fig. 27: Time variation of CDS output
Table 4: Code variation of CDS output

<table>
<thead>
<tr>
<th>Case</th>
<th>Simulated code variation (code)</th>
<th>Measured code variation (code)</th>
<th>Contributed code variation (code)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurement setup (offset of oscilloscope)</td>
<td>N/A</td>
<td>0.80 (estimated)</td>
<td>N/A</td>
</tr>
<tr>
<td>Only ramp generator operating (intrinsic noise)</td>
<td>0.23</td>
<td>1.00 (estimated)</td>
<td>0.20</td>
</tr>
<tr>
<td>CDS ADC circuit operating (power line noise)</td>
<td>0.28 (Max 0.43)</td>
<td>1.25</td>
<td>0.25</td>
</tr>
<tr>
<td>On-chip digital noise source operating (on-chip substrate noise)</td>
<td>N/A</td>
<td>3.06</td>
<td>1.81</td>
</tr>
</tbody>
</table>

Under dark illumination (i.e. pixel signal does not change), the plots of the time variation of the CDS output is obtained as shown in Fig. 27. The time variation of the CDS output when the CDS is operating is 104.0 ns that corresponds to 1.25 code as shown in Fig. 27(a). When the on-chip digital noise source is operating, the code variation rose to 3.06 code as shown in Fig. 27(b).

The simulation results and measurement results of the CDS output variation are summarized in Table 4. The code variation that is contributed from each block is obtained by the difference of the measured code variation in each case. Table 4 shows that substrate noise is the most critical noise source of the ramp signal noise when it is compared with other noise sources as mentioned above.

Conclusions:

Noise in the ramp signal fed to the CDS/ADC circuit in the CIS has the different amount of the effect on output images according to its frequency. Because the ramp signal is referenced only when the pixel signal voltage is sampled and when the output voltage of the CDS circuit crosses a switching threshold voltage of an inverter, the ramp signal is sampled into capacitors in discrete time manner and the amount of H-line noise generated in output images is strongly influenced by the sampled interval of the ramp signal.

Because the time duration between two times of sampling of the ramp signal is an order of 10 µs to 100 µs, the ramp signal noise frequency of the maximum effect is varying from 10 kHz to 100 kHz according to the pixel value of the output image. Since the fundamental frequency of the ramp signal is around this frequency range, noise filtering in the ramp signal by using band-/low-pass filter is impossible.

Also, in this paper, various sources of the ramp signal noise which mainly causes the H-line noise are analyzed, and the measurement results of the fabricated chip are provided. Measurement results show that harmonics of the digital clock by substrate noise has an effect on the ramp signal noise and then the code variation of the CDS output occurs as 1.81 code error.

Therefore, to reduce the ramp signal noise which causes H-line noise, not only a well-designed ramp generator with low noise should be considered from the early phase of design, but the substrate noise in the ramp generator should be suppressed by various circuit design techniques.

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References


