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Research Article

Self-organized methods used to fabricate nickel nano-dots on semiconductor substrates

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ABSTRACT

In this work, the nickel nano-dots were formed on different substrates such as GaN/sapphire and GaN/Si. GaN material was grown on sapphire and Si (111) wafers by Metalorganic Chemical Vapor Deposition (MOCVD). There are two self-organized methods to form Ni nano-dots. The first method used a porous alumina mask with the thickness of about 400 nm, created by the anodization process, on the top surface of the sample to allow Ni get into the bottom of the holes by electron beam evaporation. Ni nano-dots were left on the GaN surface after the mask was removed by wet etching. The second method is to anneal thin Ni film coated on the substrate by e-beam evaporation. The Ni films were performed with different annealing temperatures and times by a tube furnace. The results of both methods were investigated by FESEM. The images showed that the dot sizes varied from 69 nm to 79 nm for the first method and from 90 nm to 180 nm for the second one.

Key words: Self-organize, Nano-dots, Annealing, porous alumina

INTRODUCTION

There are many ways to fabricate nano-dots of different materials which depend on their applications to obtain better electrical and optical properties comparing to those of bulk materials [1-4]. Especially, development of low-dimensional structure of either metal or polymer used as a pattern on a semiconductor substrate such as Si and Sapphire is considerably interested. Self-organization growth and lithographic technique are widely used. Quantum dots (QDs) such as GaN or InGaN is produced by using the self-organized method with a surfactant [5] and without a surfactant [6] or by taking the advantages of the Stranski-Krastanov (S-K) growth mode [7].

Conventional patterning by lithographic techniques can be applied to the III-nitrides, such as optical lithography, holography, x-ray lithography, electron-beam lithography, and focused ion beam lithography [8]. One such advantage is that QDs can be created with specific shapes, size and arrangements. However, both lithographic technique and self-organization methods have their own drawbacks. The throughput of lithographic techniques is low and generally only small areas can be patterned. In addition, high resolution lithographic equipment is very expensive. In the case of the self-

organization growth method, there are a few types of state-of-the-art instruments such as Molecular Beam Epitaxy (MBE) [9] and Metal-Organic Chemical Vapor Deposition (MOCVD) [10] introduced to fabricate nano-pattern arrays on the surface of semiconductor surfaces. However, these instruments are designed to grow high quality of epitaxial layers rather than self-ordered nano-pattern arrays such as quantum dots or quantum wires which are non-uniform patterns.

In this work, we focus on the methods to get nano-dots by using uncomplicated techniques, low cost and high throughput to fabricate self-ordered over large areas with relatively inexpensive equipment. The first technique used to obtain nano-dots is based on a self-ordered alumina membrane directly produced on a template [11,12] and the second technique is annealing very thin Ni film to become Ni nano-dots at a particular condition [13,14]. Field emission scanning electron microscopy (FESEM) is introduced in this work.

Materials And Methods

2.1 Epitaxial growth of GaN templates on Sapphire and Si (111) substrates:

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The GaN epilayer was grown on a sapphire (0001) substrate by MOCVD machine using a two-step process. Trimethylgallium (TMGa) and NH_3 are used as the Ga and N sources, respectively. The technique uses a low-temperature GaN nucleation layer on the sapphire substrate, followed by $\sim 1.5 \mu\text{m}$ GaN growth at high temperature (figure 1(a)). In case

of Si (111), there are two layers of AlN as a buffer layer with the thickness of 40 nm and then 30 nm GaN layer at 1020°C and 200 mbar (figure 1(b)). During the growth of AlN, Al was deposited for a few seconds to prevent the surface from nitridation before switching in ammonia.

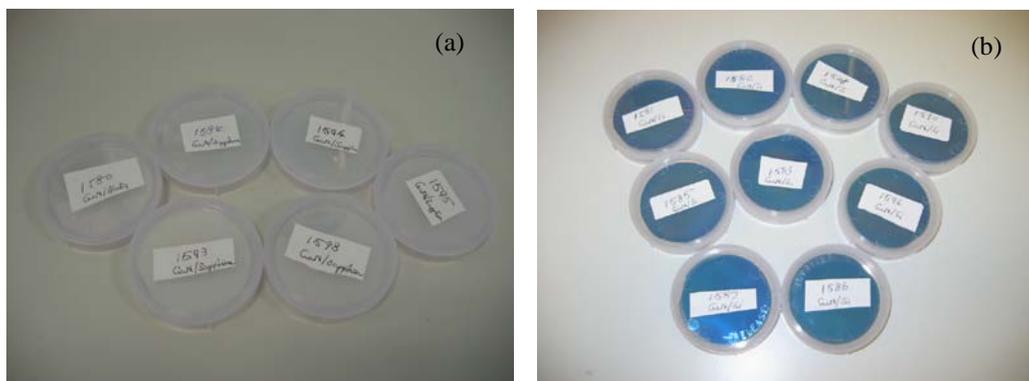


Fig. 1: GaN template on Sapphire (a) and Si (b) substrates

2.2 Fabrication of Ni nano-dot arrays:

To obtain Ni nano-dots on sapphire substrate by the first method, we used porous alumina as a nano-pattern which was directly converted from thin Al film deposited by electron beam evaporation. The fabrication processes involve: (a) depositing Ti (99.99%) and then Al (99.999%) by electron beam evaporation on the template of the semiconductor layer structure; (b) anodizing the Al to form high density nano-masks; (c) removing the bottom layer in 5% H_3PO_4 at 35°C for 15 minutes; (d) depositing Ni into the nanoholes of alumina; (e) removing the alumina mask in a mixture of H_3PO_4 and H_2CrO_4 for 30 minutes at 60°C .

The second technique is annealing thin Ni film deposited by e-beam evaporation on sapphire and Si substrates. The procedures compose of (a) depositing

SiO_2 by PECVD on both substrates, (b) depositing thin Ni material on the dielectric layer, and (c) annealing the Ni under N_2 ambient at different temperatures and times.

Field-emission scanning electron microscopy (FESEM) was used to study the morphology of Ni nano-dot arrays which was investigated on both cross-section and plan-view.

Results And Discussion

3.1 Surface of GaN template on sapphire and Si substrates:

After growing GaN templates, they were investigated by AFM for sapphire substrate and by SEM for Si substrate to see the surface morphology and to get the roughness.

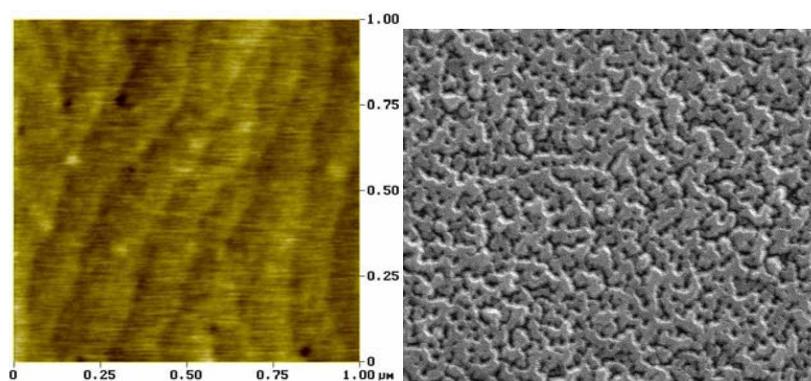


Fig. 2: (a) AFM image of GaN on sapphire (b) SEM image of GaN on Si

Figure 2(a) shows the terraces of GaN on the substrate. The roughness of the GaN surface is 0.121

nm. Figure 2(b) is SEM image of GaN on Si which has AlN as the buffer layer. Total thickness of nitride template is about 70 nm. As the SEM result, it is found that nitride layer is still not fully coalesced but it is not affected to fabricate Ni nano-dot arrays in our research.

3.2 Porous alumina on GaN template:

High purity Ti (99.99%) film was deposited and followed with Al (99.999%). The aims of depositing

Ti are to improve the adhesion of Al on the template and to make sure the Al can entirely become porous alumina because the current still apply to the process and carry on the anodization process until ended. The thickness of Ti and Al are about 10 nm and 1000 nm, respectively.

Figure 3 shows the grain sizes of the Al film. The thin material consists of different grain sizes and orientations, which range around 50 nm in size. Moreover, the film which was deposited by e-beam evaporation appears to be polycrystalline.

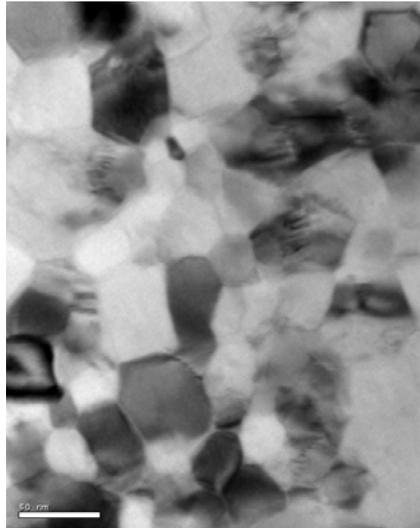


Fig. 3: TEM image of pure Al film

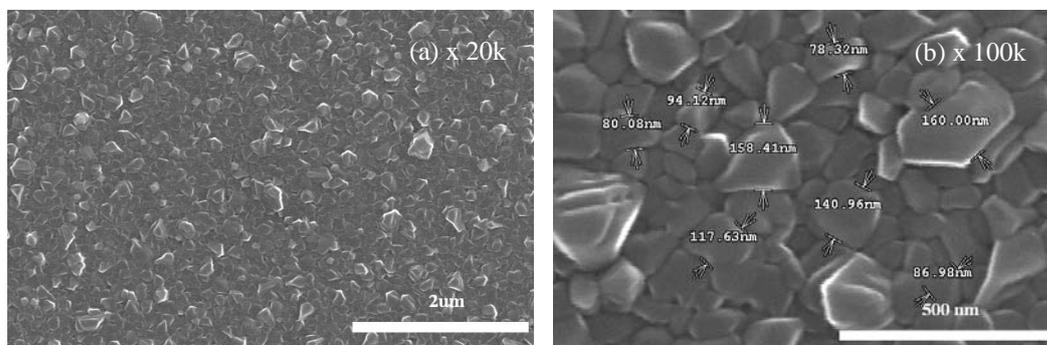


Fig. 4: Initial surface of Al film

Figure 4 shows the initial surface which consists of small grains with different sizes, as shown in Figure 4 (b) but the surface is smooth enough to do the anodization.

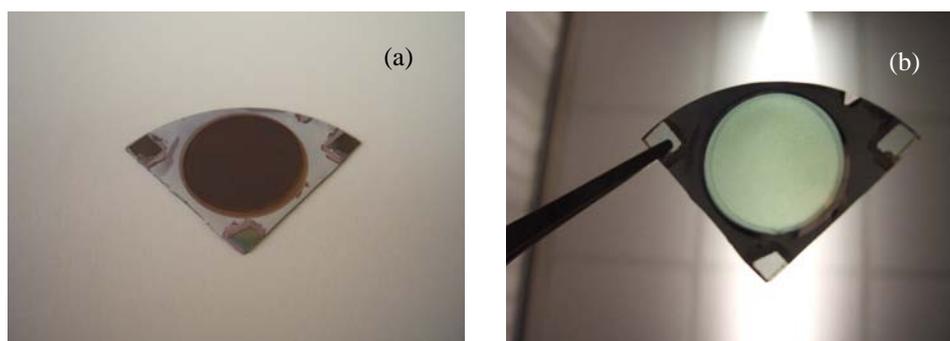


Fig. 5: Thin porous alumina film on GaN template

Figure 5 shows the porous alumina film after two step anodisation process. We found that the alumina is transparent and clear when we saw it in

the other side as shown in Figure 5 (b). Moreover, we also saw the English characters through the alumina film (no Figure here).

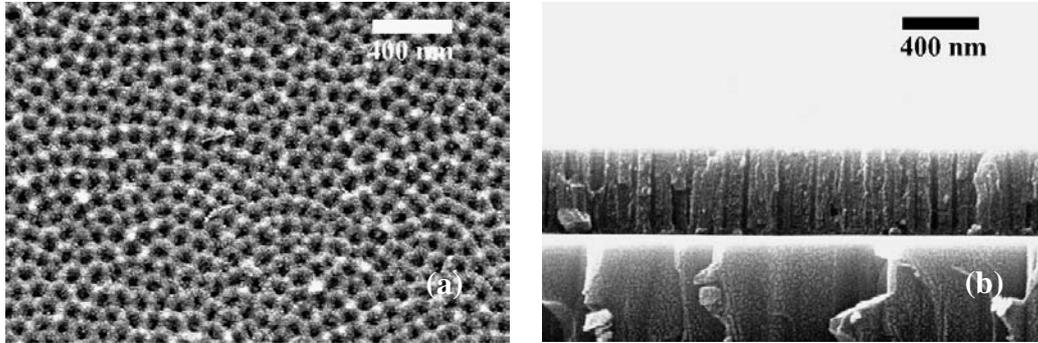


Fig. 6: Sample with thin porous alumina film on GaN template

Figure 6 shows thin alumina film which is the first step of anodisation taken for ~ 20 min, removing aluminum oxide of the first step for 8 min,

and the second step of anodisation taken for ~ 9 min to obtain the film with the thickness of 400 nm as the cross section is shown in Figure 6 (b).

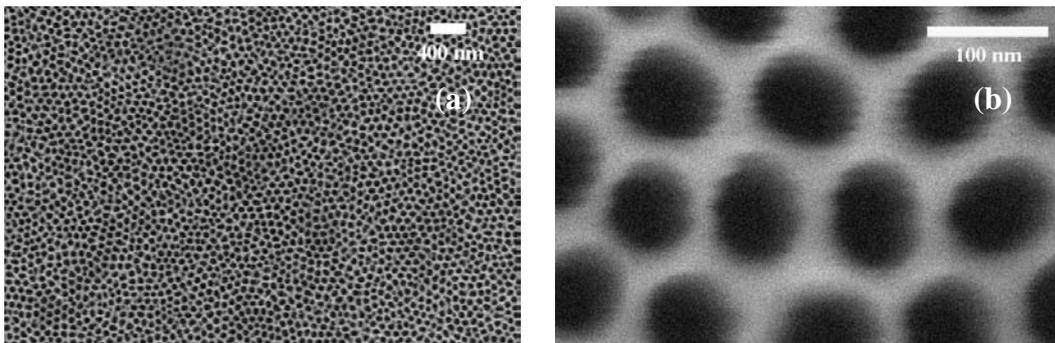


Fig. 7: Widening the pores and removing the bottom layer of the porous alumina in 5% H_3PO_4

The pores of alumina film were widening in 5% H_3PO_4 at 35°C for 18 min and also the bottom layer was removed simultaneously. It was found that the

pore size was enlarged to have the diameter of nearly about 100 nm as shown in Figure 7 (b).

3.3 Ni nano-dots using the porous alumina film:

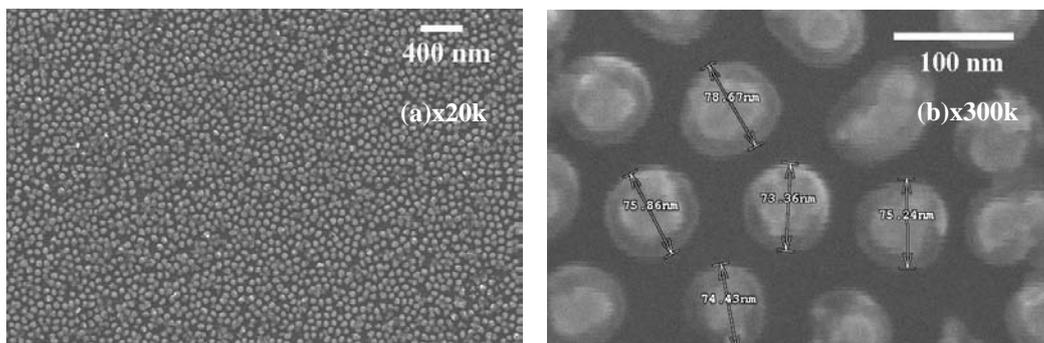


Fig. 8: Ni nano-dots by using the porous alumina mask

Ni nano-dots were formed by using the alumina mask to control the Ni vapor which deposited into the holes at the interface between the mask and GaN template. After that, the alumina mask was removed in a solution of 0.4 M H_3PO_4 + 0.2 M H_2CrO_4 at 60°C for 35 min. The Ni dots were left on the GaN surface as shown in Figure 8. The dot sizes are slightly bigger or smaller than 76 nm as shown in Figure 8 (b). Figure 8 (a) shows the Ni dots are over the whole GaN surface.

3.3 Ni nano-dots by annealing method:

In this case, the Ni dots can be fabricated on both substrates (sapphire and Si) by annealing. Prior to annealing, the dielectric layer such as SiO_2 or Si_3N_4 was coated on the template with the thickness of ~ 200 nm to prevent Ni to react with GaN surface to be nickel-gallide at high temperature [13, 14] as shown in Figure 9.

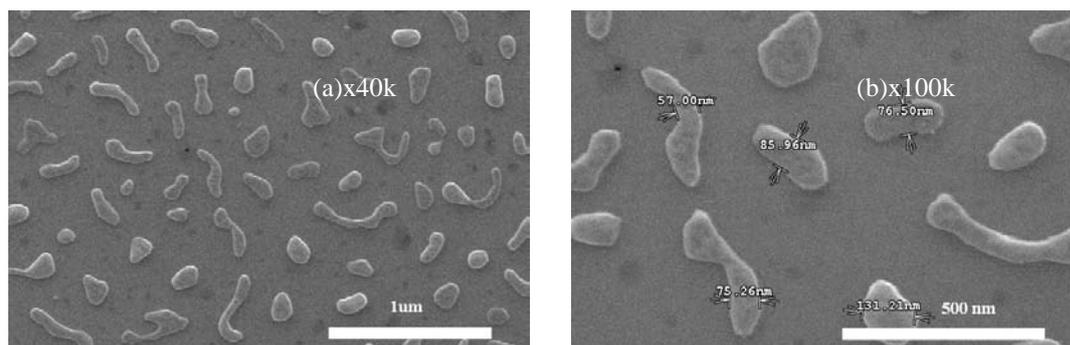


Fig. 9: SEM images after annealing thin Ni film with the dielectric layer (sapphire)

After coating SiO_2 , Ni material was deposited on the top with the thickness of 5 nm. The annealing results with different temperature conditions and time showed that the SiO_2 layer of the samples annealed at high temperature such as 845°-850°C and longer annealing time was cracked and lifted off

from the GaN template. However, it has to be compromised between the temperature and time to obtain high density Ni dots over the whole surface as shown in Figure 10 (a). The Ni dot density is ~ $2.23 \times 10^9 \text{ cm}^{-2}$.

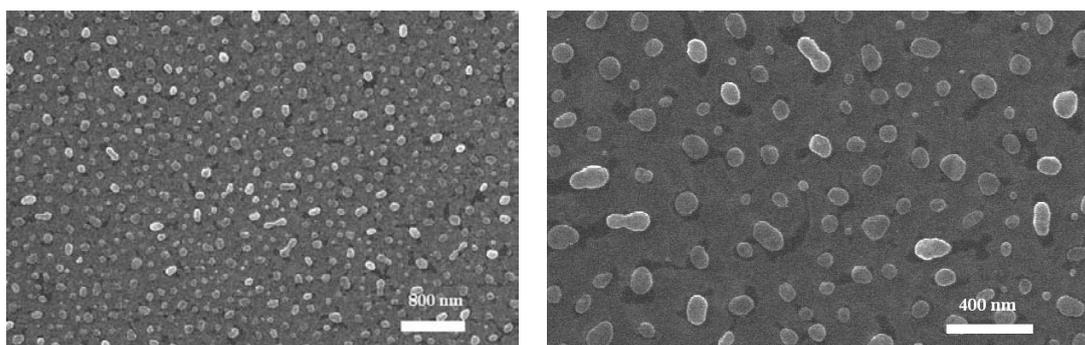


Fig. 10: Ni dots formed at 845°C for 45 sec (sapphire)

In case of thinner SiO_2 layer (140 nm), Ni thickness is still the same (5 nm). The annealing temperature was kept at 845°C and annealing time should be about 30 – 40 min less than the previous work. Figure 11 (a) and (b) showed that the Ni dots on the whole surfaces which were annealed for 30 min and 40 min, respectively. The Ni dot density of Figure 11 (b) is ~ $2.26 \times 10^9 \text{ cm}^{-2}$.

The final case is the formation of Ni dots on the Si substrate. As the results of previous works, we

started the experiment with the same conditions such as temperature and time. Our results show that the temperature is too high and the annealing time is still too long. This is because the types of substrate affected the heat transfer into sapphire and Si in different conduction rates. We found that the Si can be absorbed heat faster than the sapphire. At room temperature, the thermal conductivities of sapphire and Si are 42 W/m.K and 156 W/m.K, respectively. SiO_2 was deposited with the thickness of 250 nm on

the GaN template but the Ni thickness is still the same (5 nm).

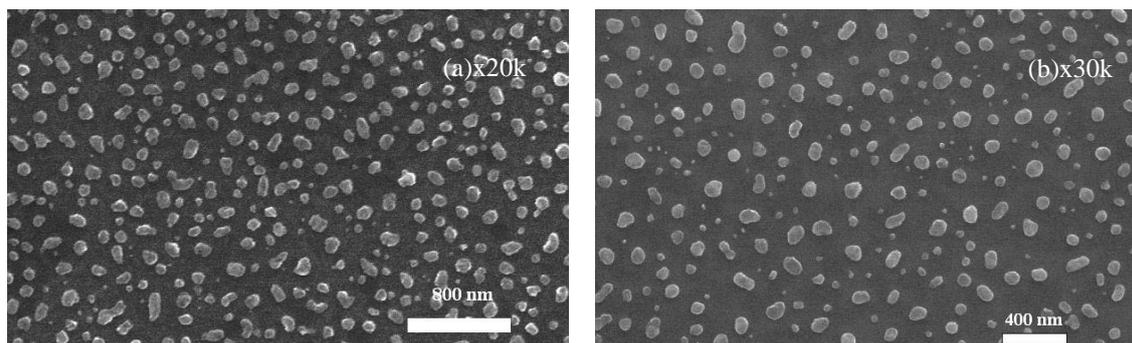


Fig. 11: Ni dots formed at 845°C for (a) 30 sec and (b) 40 sec (sapphire)

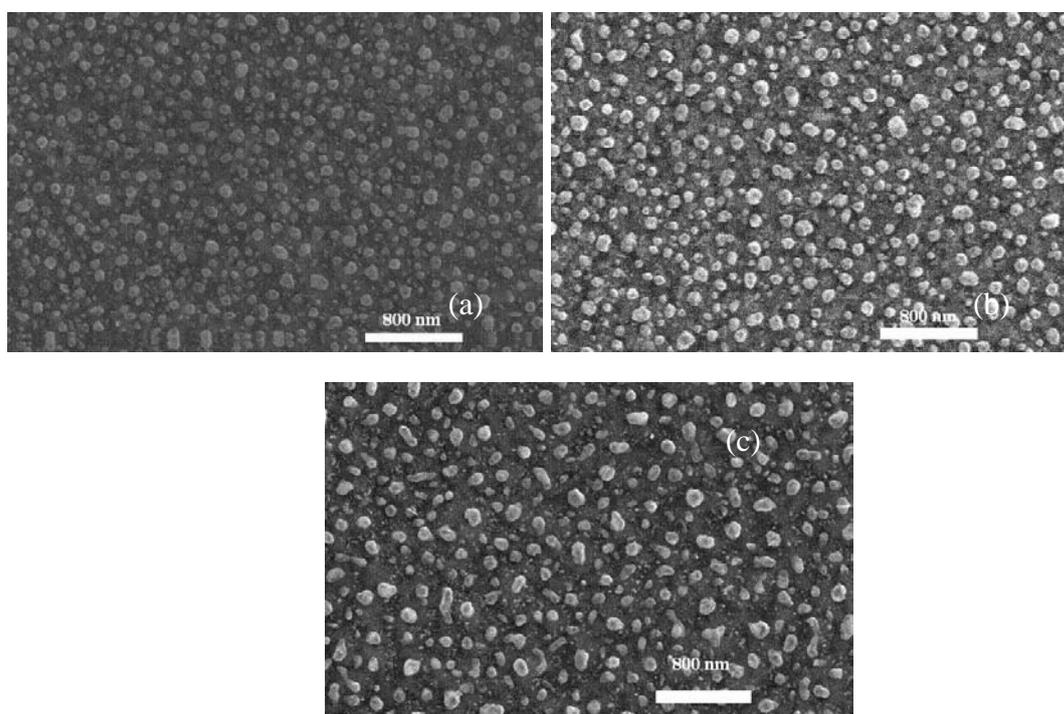


Fig. 12: Ni dots formed on the GaN template at 800°C with different annealing time (a) 30 sec (b) 31 sec (c) 33 sec (Si substrate)

Figure 12 shows the Ni dots on GaN/Al/Si. The annealing times are slightly different (30, 31 and 33 sec) at the same temperature of 800°C. The Ni dot densities of image (a), (b) and (c) are $5.06 \times 10^9 \text{ cm}^{-2}$, $3.56 \times 10^9 \text{ cm}^{-2}$ and $2.66 \times 10^9 \text{ cm}^{-2}$, respectively. The dot density of Ni on Si is higher than that of Ni on sapphire at lower annealing temperature. This confirms that Ni dots on Si substrate is formed easier and smaller and denser due to a much higher thermal conductivity led to uniformly transfer heat over the whole substrate. The nano-dot sizes fabricated by annealing method are varied from 90 to 180 nm on both substrates.

Conclusion:

This research reports the methods to fabricate Ni nano-dots with high densities without using state-of-the-art equipment. It is high throughput, low cost and uncomplicated procedure by using self-organized porous alumina mask and annealing methods. Thin alumina mask was directly fabricated on the GaN template with the thickness of ~ 400 nm. Each channel of the mask controlled the Ni vapor get down to the interface between the mask and the GaN surface. Ni dot array was formed over the whole surface after lifting off the mask in the solution of 0.4 M H_3PO_4 + 0.2 M H_2CrO_4 at 60°C for 35 min. The Ni dot sizes by this method are not much different in the range from 69 to 76 nm. The second method is annealing thin Ni film (5 nm) in the tube furnace at 845°C for 45 sec or slightly quicker which depends

on the thickness of the dielectric layer (SiO_2) on sapphire substrate. On the other hand, the formation of Ni dots on Si substrate was performed with different conditions due to much higher thermal conductivity. The annealing temperature and times are 800°C and 30-33 sec, respectively. The thickness of SiO_2 on Si substrate was kept constant of 250 nm. On both substrates, the dot sizes are varied from 90 to 180 nm.

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