ORIGINAL ARTICLES

BOE-Based Polysilicon Wire Trimming Using Oxidation Furnace

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ABSTRACT

An intensive research on nanowire structures fabrication still on going until now and have drawn attention among researcher and industries sector because of exponentially growing integration densities and shrinking characteristic geometries on a chip, the wires, rather than devices. Researchers still investigate the characteristic of a nanowire and tend to develop to its full potential. Though the methods available today such as RIE and EBL are very reliable, but it were very costly and time consuming. Its processes also are a bit complicated. Hence, these study attempt to overcome these disadvantages. Thus we fabricated a poly-silicon micro wire using BOE trimming method, the result which was observed through high microscope and I-V characterization shows well reduction trend in poly-silicon wire and we further compared two oxidation method for the trimming: wet oxidation and dry oxidation, the wet oxidation gave faster trimming rate however, the good profile was obtained only with dry oxidation method. Hence we conclude that the dry oxidation can used to obtained nanowire with less <20 nm with 16 step from 1 µm because its trim about 40% in actual size of the wire in each step.

Key words: BOE; fabrication; silicon nanowire; oxidation furnace.

Introduction

Nanotechnology is very diverse, ranging from extensions of conventional device physics to completely new approaches based upon molecular self-assembly, from developing new materials with dimensions on the nanoscale to investigating whether it can be directly control matter on the atomic scale. Nanotechnology entails the application of fields of science as diverse as surface science, organic chemistry, molecular biology, semiconductor physics and microfabrication. Nanotechnology may be able to create many new materials and devices with a vast range of applications, such as in medicine, electronics, biomaterials and energy production. There are many applications where nanowires may become important in electronic, opto-electronic and nanoelectromechanical devices, as additives in advanced composites, for metallic interconnects in nanoscale quantum devices, as field-emitters and as leads for biomolecular nanosensors. This project present the fabrications of nanowire by wet etch trimming technique by using the oxidation furnace with the help of buffered oxidation etch (BOE) solution (Appenzeller, J., 2006; Sheu, J.T., 2006; Cui, Y., 2001; Patolsky, F., 2004; Zheng, G., 2005; Hong Xiao, 2001; Haruhiko Abe, 2008).

In thermal oxidation, silicon wafers are oxidized in furnaces at about 1000 °C. The furnaces consist of a quartz tube in which the wafers are placed on a carrier made of quartz glass. For heating there are several heating zones and for chemical supply multiple pipes. Quartz glass has a very high melting point (above 1500 °C) and thus is applicable for high temperature processes. To avoid cracks or warping, the quartz tube is heated slowly (e.g. +10 °C per minute) (Zheng, G., 2005; Chan, W.C.W., S.M. Nie, 1998; Adam, T., 2013; Adam, T., 2013; Adam, T., 2013; Adam, T., 2012). The tempering of the tube can be done very accurate via individual heating zones. The oxygen is led to the wafers in gaseous state and reacts at the wafer surface to form silicon dioxide. A film of glass with amorphous structure is formed. Depending on the gases different oxidations occur (a thermal oxidation has to take place on a bare silicon surface). The thermal oxidation can be divided into the dry and wet oxidation, while the latter can be divided into the wet oxidation and the H2-O2 combustion. In wet thermal oxidation, the oxygen is led through a bubbler vessel filled with heated water (about 95 °C), so that in addition to oxygen water is present in the quartz tube as steam.

Table 1: Comparisons of growth rate.

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Dry oxidation</th>
<th>Wet oxidation</th>
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<tbody>
<tr>
<td>900°C</td>
<td>19 nm/h</td>
<td>100 nm/h</td>
</tr>
<tr>
<td>1000°C</td>
<td>50 nm/h</td>
<td>400 nm/h</td>
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<tr>
<td>1100°C</td>
<td>120 nm/h</td>
<td>630 nm/h</td>
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In the beginning, the oxygen and silicon react to form silicon dioxide (Adam, T., 2012). Now the oxide layer at the surface has to be surpassed by other oxygen atoms which have to diffuse through the dioxide layer to react with the silicon crystal beneath. For this reason the growth rate primarily depends on the reaction time of oxygen and silicon, while at a certain thickness the oxidation rate is mainly determined by the velocity of diffusion of the oxygen through the silicon dioxide. With increasing thickness of the dioxide the growth rate decreases (Adam, T., 2012; Hashim, U., 2012; Al-Mufti, W.M., 2012; Adam, T., 2012). Since the layer is amorphous, not all bonds in the silicon dioxide are intact. Partial there are dangling bonds (free electrons and holes) at the interface of silicon and SiO2, and therefore there is a slightly positively charged zone at the interface. Since these charges affect the integrated circuit in a negative manner, one tries to reduce these charges (Hashim, U., 2012; Rao, B.S., 2012; Adam, T., 2012; Hashim, U., 2012). This can be done with a higher temperature during oxidation or by using the wet oxidation which causes only a light charge. Of course wet and dry oxidation cannot be exchanged arbitrarily, since electrical properties of gate oxides for example can only be fulfilled by oxides grown in dry processes (Adam, T., 2012; Hashim, U., 2012; Chee, P.S., 2012).

Fig. 1: Growth of Dioxide (Darius Andriukaitis, 2007).

The growth of silicon oxide is the reaction of surface only – after the SiO2 thickness begins to build up, the arriving oxygen molecules must diffuse through the growing silicon dioxide layer to get to the silicon surface in order to react. As a result, the chemical reaction occurs at the Si SiO2 surface. In thermal oxidation with silicon, the silicon reacts with oxygen to form silicon dioxide (Darius Andriukaitis, 2007). The ratio of the grown oxide layer and of used up silicon is 2.27, which means that the dioxide is growing into the silicon substrate by 45% of the total thickness of the dioxide (Adam, T., 2012; Hashim, U., 2012; Hashim, U., S.A.B. Ariffin, 2012).

Materials and Methodology:

The fabrication starts with preparing the materials to fabricate. After cleaning the wafer, we deposit silicon nitride and polysilicon. After that we deposit aluminium as its fourth surface. Then it is time for the photolithography process where we firstly coat the resist onto the sample and then expose the sample to the UV light to get the pattern. Then the sample undergoes development process where the sample is developed to remove unwanted resist. Afterward the sample undergoes ICP-RIE. The main of the project is the trimming process at oxidation furnace and later with the help of BOE. The sample is inspected using some measurement equipment and trimming process is repeated until it achieves desired size. The general process flow is shown in the flow chart below:

Result and Discussion

During the process, the samples were inspected using High Powered Microscope (HPM) and SEM. The samples will undergo through the trimming process at the oxidation furnace at a very high temperature. This is the main part of this project. The technique forces an oxidizing agent to diffuse into the wafer at high temperature and react with it. This is a way to produce a thin layer of silicon oxide on the surface of the silicon. Silicon oxide layer then will etched out by using BOE solution. This step eventually will reduce the size of the silicon wire. The figure 2 shows the final structure of the samples under TableTop Microscope TM3000. 180 nm of wire was obtained after 16 times of repeated trimming process at the oxidation furnace.
Fig. 2: Fabrication flow.

Fig. 3: (a) HPM image after first of the trimming process (b) HPM image after second step of the trimming process (c and d) structure of nanowire under SEM.

To check the performance of the sample, the samples need to be deposited with Aurum (Au) layer and thus patterning process first. The figures below show the structure of the sample after been deposited with desired Aurum layer. After that only the wire will be tested with electrical measurement. The sample was tested. If it has not achieved the desired size, the gold layer will be etched out and the trimming process using oxidation furnace will be repeated until it reaches the target size.
Fig. 4: The polysilicon nanowires after gold deposited and inspect using HPM (a) x5, (b) x20.

One way to test whether the nanowire is getting smaller or not is through dielectric analyzer. Based on electrical resistivity formula, resistance is directly proportional to length over area. If the area is reducing, the resistance will be increasing. One of the reasons the electrical measurement is being conducted is to check whether the wire’s size is reducing or not. Many measurements were taken after each trimming to get the data for the graph. The table 4.1 below show the equation for resistivity while figures below show the graph of current versus resistance.

Fig. 5: Graph of current versus resistance.
Based on the graphs, we can see that the resistance is getting larger and current is getting lower due to the diameter of the wire also reducing. The resistance getting higher is due to the area of the nanowire is getting smaller after each trimming. This prove that the trimming have achieved its objective of reducing the size of the nanowire. After 16 times of trimming, we finally achieved nanowire with size of 180 nm. But the trimming still needs to be continued until we reach a size of under 20nm.

Conclusion:

This project objective is to fabricate and characterize polysilicon nanowire with dimensions under 200 nm using the trimming technique. This is to prove that by using the trimming technique can also form polysilicon nanowire with dimension of nano size other than using two other methods which is e-beam lithography and spacer pattern lithography that would cost so much more. The material used in this project is polysilicon which is very commonly used in the nanotechnology. Polysilicon nanowire brings many benefits to the world today. The polysilicon nanowire represents a promising material with strong potential for a large variety of applications. Other than that, the polysilicon nanowire brings many advantages with respect to bulk silicon. It has high surface to volume ratio, giant piezoresistivity, possibility of surface functionalization, synthesis compatible with large area technology and it could lead to the development of innovative electronic devices. Polysilicon nanowire now a day many use it as a development of nanosensors with high sensitivity.

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