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# A Capacitive Loop-Connected Topology with a Large Number of DC-DC Voltage Ratios

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ABSTRACT

**Background:** The switched capacitor (SC) DC-DC converter has been widely used as a building block of portable electric devices, because the SC DC-DC converter can be designed without magnetic components. However, the SC DC-DC converter is difficult to achieve a high step-up gain and flexible conversion ratios, because the conversion ratio of the SC DC-DC converter is predetermined by the number of capacitors. **Objective:** In this paper, we propose a capacitive loop-connected topology to achieve a high step-up gain and flexible conversion ratios. Unlike the conventional series-connected converter, the proposed loop-connected converter consisting of positive/negative DC-DC converters provides the output voltage expressed as a combination of multiplication and subtraction. Furthermore, by equalizing the electric charge in parasitic capacitors, the proposed converter can reduce parasitic losses. **Results:** Concerning the simple example of the proposed converter, simulation program with integrated circuit emphasis (SPICE) simulations, theoretical analysis, and experiments were performed to clarify characteristics. The SPICE simulations showed the following results: (1) by combining positive converter blocks and negative converter blocks, the proposed converter can achieve a larger number of DC-DC voltage ratios than the conventional series-connected converter; (2) more than 5% of the power efficiency was improved by the proposed power saving technique when the output load was 10kΩ and the stray parasitic capacitance was 0.5pF; and (3) In the experimental circuit built with commercially available ICs, the measured output was about 93.7% of the ideal output voltage when the output load was 100kΩ. **Conclusion:** In this paper, we proposed a loop-connected topology of a switched capacitor converter. The conclusion of this research is as follows: (1) by combining positive converter blocks and negative converter blocks, the proposed converter can achieve a larger number of DC-DC voltage ratios than the conventional series-connected converter; (2) the proposed power saving technique can improve power efficiency effectively in the case of a small output current; and (3) the validity of the proposed circuit topology was confirmed by experiments.



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## INTRODUCTION

The switched capacitor (SC) DC-DC converter (Allasasmeh *et al.* (2010), Beck *et al.* (2011), Chang *et al.* (2011), Chang *et al.* (2011), Chen *et al.* (2011), Doms *et al.* (2009), Eguchi *et al.* (2012), Eguchi *et al.* (2004), Eguchi *et al.* (2004), Eguchi *et al.* (2011), Huang *et al.* (2012), Hwang *et al.* (2009), Ishida *et al.* (2009), Kim *et al.* (2009), and Terada *et al.* (2006)) has been widely used as a building block of portable electric devices, because the SC DC-DC converter can be designed without magnetic components. For example, Doms *et al.* (2009) designed a capacitive power management circuit by using a charge pump, Kim *et al.* (2009) realized white light emitting diode (WLED) backlights using a negative charge pump, and Ishida *et al.* proposed non-volatile memories using a positive/negative charge pump (Ishida *et al.* (2009)). Among others, an energy harvesting system utilizing SC DC-DC converters (Chen *et al.* (2011) and Eguchi *et al.* (2012)) attracts many researchers' attention in recent years. Energy harvesting is the process by which energy is delivered from external sources such as thermal energy, kinetic energy, and so on, where ambient energy is converted into electrical energy by energy harvesting devices. In the design of energy harvesting systems, the converter with a large number of conversion ratios and a high step-up gain is required, because electric energy produced by the energy harvesting device is small. However, the SC DC-DC converter has the drawback that conversion ratio

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cannot be changed linearly, because the conversion ratio of the SC DC-DC converter is predetermined by the number of capacitors.

To overcome above-mentioned problem, several types of efficient topologies which can achieve a large number of conversion ratios and/or a high step-up gain have been proposed in previous studies. For example, Beck *et al*. (2011) proposed a capacitive transposed series-parallel topology to realize fine tuning capabilities. The configuration of this converter is based on parallel branches of series capacitors in the charging state and series elements of parallel capacitors in the discharging state. The conventional converter (Beck *et al*. (2011)) is suitable for fine tuning in the DC-DC voltage ratios. However, Beck's converter is difficult to achieve high step-up gain in a small number of capacitors. Terada *et al*. (2006) and Eguchi *et al*. (2004) proposed cascade-connected SC DC-DC converters, and Chang *et al*. (2011) and Eguchi *et al*. (2004 and 2011) proposed series-connected SC DC-DC converters. By cascading SC DC-DC converters, the cascade-connected converter provides the sum of the output voltage of each converter. However, Terada's converter (Terada *et al*. (2006)) needs a complicated multiphase timing circuit. On the other hand, by connecting SC DC-DC converters in series, the series-connected converter (Chang *et al*. (2011) and Eguchi *et al*. (2004)) provides integral multiples of the input or integral divisions of the input. Unlike the cascade-connected converter, Chang's converter (Chang *et al*. (2011)) can be controlled by two-phase clock pulses. Nevertheless, there is still room for improvement in circuit topologies.

In this paper, we propose a capacitive loop-connected topology to realize a high step-up gain and flexible conversion ratios. Unlike conventional series-connected converters (Chang *et al*. (2011) and Eguchi *et al*. (2004)), the proposed converter consists of series-connected converters providing a positive output and series-connected converters providing a negative output. The proposed converter generates the sum of the output voltages of these series-connected converters to an output load. Therefore, the proposed converter can achieve a larger number of DC-DC voltage ratios than the conventional series-connected converter (Chang *et al*. (2011) and Eguchi *et al*. (2004)).

In the design of the proposed loop-connected converter, the charge reusing technique (Allasasmeh *et al*. (2010)) is applied to reduce parasitic power losses, because improving power efficiency is one of the most important issues in the integrated circuit (IC) design of SC DC-DC converters. The power efficiency of the SC DC-DC converter consisting of discrete components is mainly limited by capacitor charging and discharging losses and resistive conduction losses. However, the energy loss due to stray parasitic capacitances cannot be ignored in the IC design. In previous studies, Allasasmeh *et al*. (2010) applied a charge reusing technique for a charge pump, a heap converter, and a Fibonacci converter. However, the charge reusing technique has not been applied for negative DC-DC converters in previous studies (Hwang *et al*. (2009), Allasasmeh *et al*. (2010), and Huang *et al*. (2012)). In the design of the proposed converter, the charge reusing technique is applied for not only the positive converter block but also the negative converter block.

To confirm the validity of the proposed converter, simulation program with integrated circuit emphasis (SPICE) simulations, theoretical analysis, and experiments are performed.

*Circuit structure:*

*Conventional Converter:*

Figure 1 shows the conventional series-connected converter (Chang *et al*. (2011) and Eguchi *et al*. (2004)). Since the converter block of Figure 1 (b) is a series-parallel type converter proposed by Ueno *et al*, the conversion ration $\gamma_i$ ($i$=1, …, $R$) of the $i$-th converter block is $m$ or 1/$m$ ($m$=1, …, $N$). The series-parallel type converter of Figure 1 (b) consists of 3$N$+1 switches and $N$ capacitors. Table 1 shows the timing of clock pulses for Figure 1 (b). As Table 1 shows, the MOS switch is driven by non-overlapped two-phase pulses. By connecting series-parallel type converters, the conventional converter provides the following output voltage:

$$V_{out} \cong \prod_{k=1}^{R} \gamma_k V_{in}. \tag{1}$$

As (1) shows, the series-connected topology of the conventional converter provides integral multiples of the input or integral divisions of the input. Concretely, the output voltage of the conventional converter is $V_{out}$={(1/4)$V_{in}$, (1/2)$V_{in}$, $V_{in}$, 2$V_{in}$, 4$V_{in}$} when the parameters $R$ and $N$ are two (i.e. $\gamma_k$ ={1/2, 1, 2}). Although the conventional topology can achieve a high step-up gain, there is still room for improvement.

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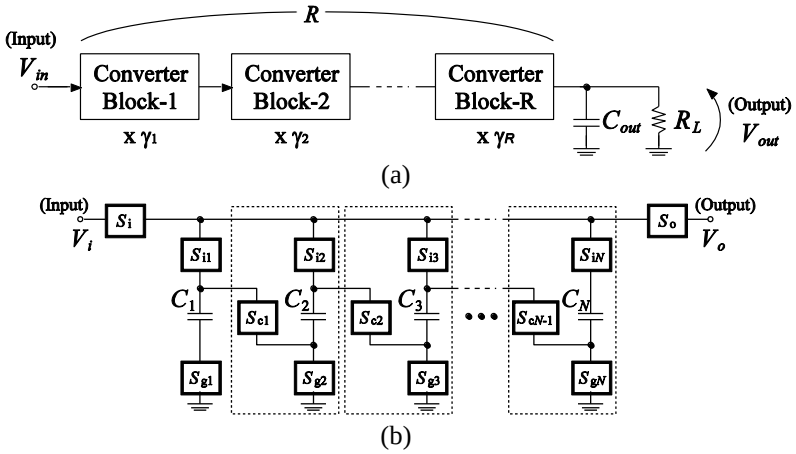



**Fig. 1:** Conventional converter using series-parallel converters, (a) Block diagram and (b) Converter block.

**Table 1:** Timing of clock pulses for the series-parallel converter.

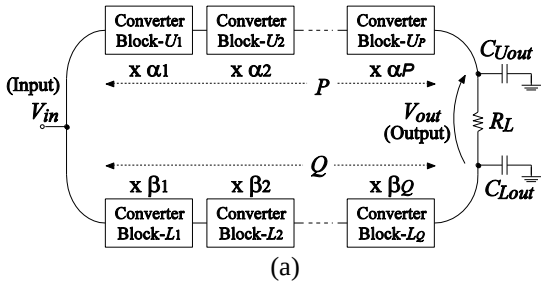
| Conversion Mode | State | On | Off |
|---|---|---|---|
| Up | $T_1$ | $S_i$, $S_{g1}$,…, $S_{gN}$, $S_{i1}$,…, $S_{iN}$ | $S_o$, $S_{g1}$, $S_{iN}$, $S_{c1}$,…, $S_{cN-1}$ |
| | $T_2$ | $S_o$, $S_{g1}$, $S_{iN}$, $S_{c1}$,…, $S_{cN-1}$ | $S_i$, $S_{g1}$,…, $S_{gN}$, $S_{i1}$,…, $S_{iN}$ |
| Down | $T_1$ | $S_i$, $S_{iN}$, $S_{g1}$, $S_{c1}$,…, $S_{cN-1}$ | $S_o$, $S_{g1}$,…, $S_{gN}$, $S_{i1}$,…, $S_{iN}$ |
| | $T_2$ | $S_o$, $S_{g1}$,…, $S_{gN}$, $S_{i1}$,…, $S_{iN}$ | $S_i$, $S_{iN}$, $S_{g1}$, $S_{c1}$,…, $S_{cN-1}$ |

*Proposed Converter:*

Figure 2 shows the proposed loop-connected converter. As Figure 2 (a) shows, the proposed converter consists of converter block-$U_i$ ($i$=1, …, $P$) and converter block-$L_j$ ($j$=1, …, $Q$), where $\alpha_i$ ($i$=1, …, $P$) and $\beta_j$ ($j$=1, …, $Q$) are conversion ratios. The circuit structure of these converter blocks is shown in Figure 2 (b) and (c). By combining these blocks, the proposed loop- connected converter is synthesized. Table 2 shows the timing of clock pulses for the positive converter block. By controlling MOS switches as shown in Table 2, $m$ times or 1/$m$ times conversion ($m$=1, …, $N$) is achieved by the positive converter block. On the other hand, Table 3 shows the timing of clock pulses for the negative converter block. By controlling MOS switches as shown in Table 3, -$m$ times or -1/$m$ times conversion is achieved by the negative converter block. As Tables 2 and 3 show, the switch $S_e$ is turned on at State-$T_2$ and $T_4$ to equalize the electric charge stored in stray parasitic capacitances $C_t$ and $C_b$. By equalizing the electric charge stored in $C_t$ and $C_b$, parasitic energy loss caused by $C_t$ and $C_b$ is reduced. The output voltage of the proposed converter is expressed as

$$V_{out} \cong \left( \prod_{i=1}^{P} \alpha_i - \prod_{j=1}^{Q} \beta_j \right) V_{in}, \tag{2}$$

where the parameters $\alpha_i$ and $\beta_i$ are conversion ratios. As (1) and (2) show, the proposed converter can achieve higher step-up gain and more flexible conversion ratios, because the output voltage of (2) is equal to that of (1) in the case that $\alpha_i$ =0 and $P$=1. Concretely, the output voltage of the proposed converter is $V_{out}$={ ± (1/4)$V_{in}$, ± (1/2)$V_{in}$, ± $V_{in}$, ± (3/2)$V_{in}$, ± 2$V_{in}$, ± (5/2)$V_{in}$, ± 3$V_{in}$, ± 4$V_{in}$} when the parameters $N$ and $P$+$Q$ are two (i.e. $\alpha_i$ =$\beta_i$ ={-2, -1, -1/2, 1/2, 1, 2}).



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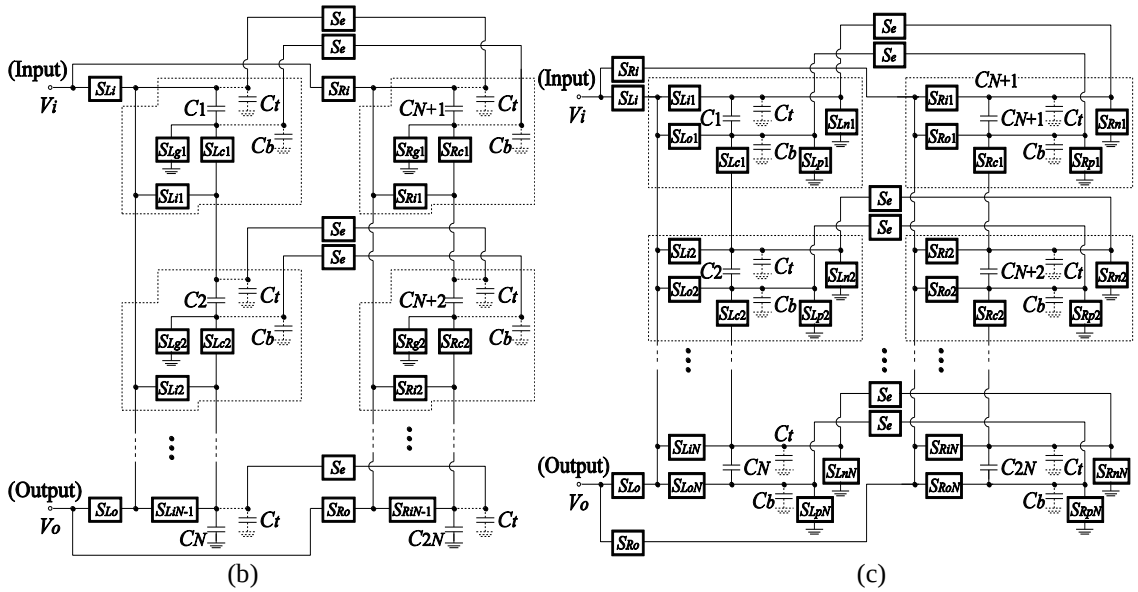


**Fig. 2:** Proposed loop-connected converter, (a) Block diagram, (b) Positive converter, and (c) Negative converter.

*Theoretical Analysis:*

To estimate characteristics of the proposed loop-connected converter, theoretical analysis is performed concerning maximum efficiency and a maximum output voltage. The theoretical analysis is performed under the conditions: 1) Parasitic elements are negligibly small; 2) MOS switch is modeled by an ideal switch with on-resistance $R_{on}$; and 3) Time constant is much larger than the period of clock pulse $T$.

*Positive Converter Block:*

Figure 3 shows the instantaneous equivalent circuits of the positive converter block, where $R_{on}$ is an on-resistance of the MOS switch. In steady state, the differential value of the electric charge in capacitor $C_n$ ($n$=1, …, 2$N$) satisfies

$$\sum_{i=1}^{4} \Delta q_{T_i}^{n} = 0, \tag{3}$$

**Table 2:** Timing of clock pulses for the positive converter block.

| Mode | State | On | Off |
|---|---|---|---|
| Up | $T_1$ | $S_{Li}, S_{Lg1},\ldots, S_{LgN-1}, S_{Li1},\ldots, S_{LiN-1}, S_{Ro}, S_{Rc1},\ldots, S_{RcN-1}$ | Other switches |
| | $T_3$ | $S_{Ri}, S_{Rg1},\ldots, S_{RgN-1}, S_{Ri1},\ldots, S_{RiN-1}, S_{Lo}, S_{Lc1},\ldots, S_{LcN-1}$ | Other switches |
| | $T_2$ , $T_4$ | $S_e$ | Other switches |
| Down | $T_1$ | $S_{Li}, S_{Lc1},\ldots, S_{LcN-1}, S_{Ro}, S_{Rg1},\ldots, S_{RgN-1}, S_{Ri1},\ldots, S_{RiN-1},$ | Other switches |
| | $T_3$ | $S_{Ri}, S_{Rc1},\ldots, S_{RcN-1}, S_{Lo}, S_{Lg1},\ldots, S_{LgN-1}, S_{Li1},\ldots, S_{LiN-1},$ | Other switches |
| | $T_2$ , $T_4$ | $S_e$ | Other switches |

**Table 3:** Timing of clock pulses for the negative converter block.

| Mode | State | On | Off |
|---|---|---|---|
| Up | $T_1$ | $S_{Li}, S_{Lp1},\ldots, S_{LpN}, S_{Li1},\ldots, S_{LiN}, S_{Ro}, S_{Rc1},\ldots, S_{RcN-1}, S_{Rn1}, S_{RoN}$ | Other switches |
| | $T_3$ | $S_{Ri}, S_{Rp1},\ldots, S_{RpN}, S_{Ri1},\ldots, S_{RiN}, S_{Lo}, S_{Lc1},\ldots, S_{LcN-1}, S_{Ln1}, S_{LoN}$ | Other switches |
| | $T_2$ , $T_4$ | $S_e$ | Other switches |
| Down | $T_1$ | $S_{Li}, S_{Li1}, S_{Lc1},\ldots, S_{LcN-1}, S_{LpN}, S_{Rn1},\ldots, S_{RnN}, S_{Ro1},\ldots, S_{RoN}, S_{Ro}$ | Other switches |
| | $T_3$ | $S_{Ri}, S_{Ri1}, S_{Rc1},\ldots, S_{RcN-1}, S_{RpN}, S_{Ln1},\ldots, S_{LnN}, S_{Lo1},\ldots, S_{LoN}, S_{Lo}$ | Other switches |
| | $T_2$ , $T_4$ | $S_e$ | Other switches |

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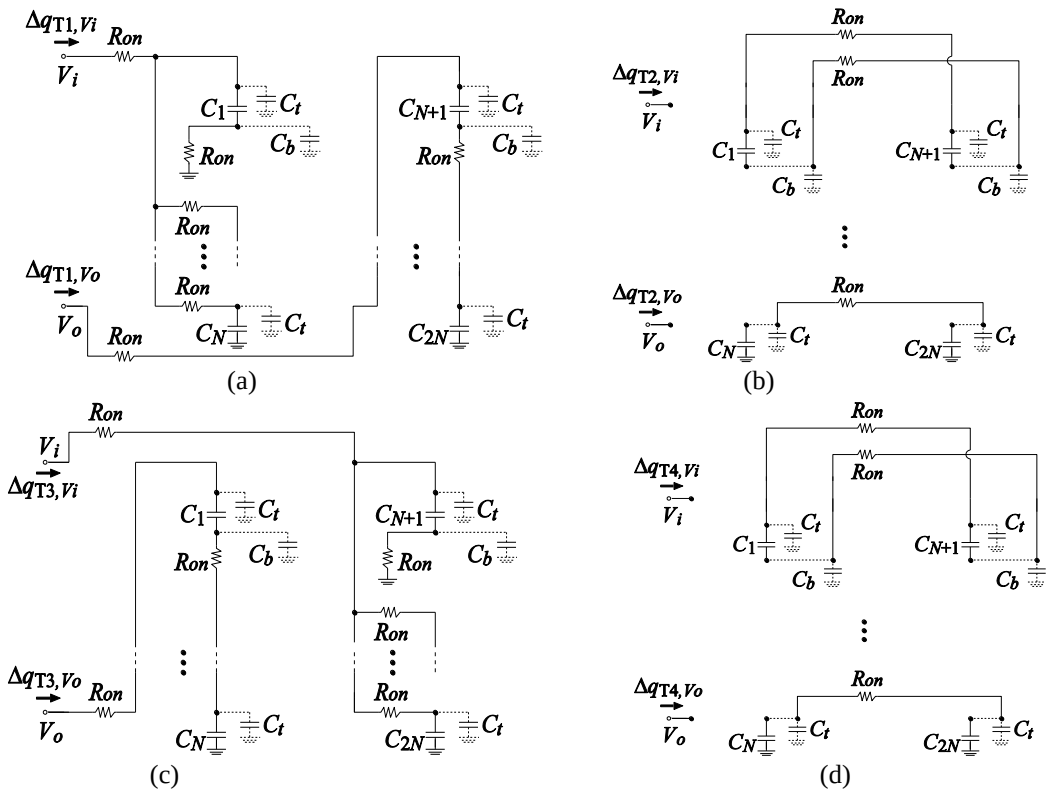


**Fig. 3:** Instantaneous equivalent circuits of the positive converter block in the case of step-up conversion.

where $T=\sum_{i=1}^{4}T_i,\ T_1=T_3=\left(\frac{1-2\delta}{2}\right)T,$ and $T_2=T_4=\delta T$.

In (3), $\Delta q_{Ti}{}^n$ denotes the electric charge of the $n$-th capacitor in the case of State-$T_i$ and $\delta$ is the parameter to determine the interval of $T_2$ and $T_4$. In the case of the step-up mode, the differential values of the electric charge in terminal $V_i$ and terminal $V_o$, $\Delta q_{Ti,Vi}$ and $\Delta q_{Ti,Vo}$, are obtained by the following equations:

*State-$T_1$*: $\Delta q_{T_1,V_i}=\sum_{k=1}^{N}\Delta q_{T_1}^{k}$ and $\Delta q_{T_1,V_o}=\Delta q_{T_1}^{N+1}=\cdots=\Delta q_{T_1}^{2N}$ (4)

*State-$T_2$*: $\Delta q_{T_2,V_i}=\Delta q_{T_2,V_o}=0$ and $\Delta q_{T_2}^{n}=0$ (5)

*State-$T_3$*: $\Delta q_{T_3,V_i}=\sum_{l=N+1}^{2N}\Delta q_{T_3}^{l}$ and $\Delta q_{T_3,V_o}=\Delta q_{T_3}^{1}=\cdots=\Delta q_{T_3}^{N}$ (6)

*State-$T_4$*: $\Delta q_{T_4,V_i}=\Delta q_{T_4,V_o}=0$ and $\Delta q_{T_4}^{n}=0$ (7)

Using (3) - (7), the average input current and the average output current can be expressed as

$$\overline{I_i}=\frac{1}{T}\left(\sum_{i=1}^{4}\Delta q_{T_i,V_i}\right)=\frac{\Delta q_{V_i}}{T},\quad \text{and} \quad \overline{I_o}=\frac{1}{T}\left(\sum_{i=1}^{4}\Delta q_{T_i,V_o}\right)=\frac{\Delta q_{V_o}}{T}, \tag{8}$$

where $\Delta q_{Vi}$ and $\Delta q_{Vo}$ are the electric charges in terminal $V_i$ and terminal $V_o$, respectively. Substituting (3)-(7) into (8), we have the relation between the average input current and the average output current as follows:

$$\overline{I_i}=-N\overline{I_o},\quad \text{where} \quad \Delta q_{V_i}=2N\Delta q_{T_1}^{1},\ \text{and}\ \Delta q_{V_o}=-2\Delta q_{T_1}^{1}. \tag{9}$$

Next, let us consider the consumed energy in one period. In Figure 3, the consumed energy can be expressed as

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$$W_T = \sum_{i=1}^{4} W_{T_i}, \tag{10}$$

where $$W_{T_1} = \sum_{k=2}^{N-1} \frac{2R_{on}}{T_1}\left(\Delta q_{T_1}^{k}\right)^2 + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^{1}\right)^2 + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^{N}\right)^2 + \frac{R_{on}}{T_1}\left(\sum_{k=1}^{N}\Delta q_{T_1}^{k}\right)^2 + \frac{NR_{on}}{T_1}\left(\Delta q_{T_1}^{N+1}\right)^2$$
$$= \frac{\{2(N-1)+N^2+N\}R_{on}}{DT}\left(\Delta q_{T_1}^{1}\right)^2,$$

$W_{T_3} = W_{T_1}$, and $W_{T_2} = W_{T_4} = 0$,

because the converter block has bilateral symmetry. Therefore, we have the consumed energy as follows:

$$W_T = \frac{\{2(N-1)+N^2+N\}R_{on}}{(1-2\delta)T}\left(\Delta q_{V_o}\right)^2. \tag{11}$$

Here, in the general equivalent circuit of SC power converters (Eguchi *et al*. (2011) and (2012)), $W_T$ can be defined as

$$W_T := \left(\frac{\Delta q_{V_o}}{T}\right)^2 \cdot R_{SC} \cdot T, \tag{12}$$

where $R_{SC}$ is called the SC resistance. Therefore, from (11) and (12), the SC resistance in the case of the step-up conversion can be obtained as

$$R_{SC} = \frac{(N^2+3N-2)R_{on}}{1-2\delta}. \tag{13}$$

By combining (9) and (13), we have the equivalent circuit in the case of the step-up conversion as follows:

$$\begin{bmatrix} \overline{V_i} \\ \overline{I_i} \end{bmatrix} = \begin{bmatrix} \frac{1}{N} & 0 \\ 0 & N \end{bmatrix} \begin{bmatrix} 1 & R_{SC} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_o} \\ -\overline{I_o} \end{bmatrix}, \tag{14}$$

because it is known that the general equivalent circuit of SC power converters can be expressed by the Kettenmatrix (Eguchi *et al*. (2011) and (2012)).

On the other hand, the equivalent circuit in the case of the step-down conversion can be obtained by the same method. In the case of the step-down conversion, the equivalent circuit can be expressed by the following determinant:

$$\begin{bmatrix} \overline{V_i} \\ \overline{I_i} \end{bmatrix} = \begin{bmatrix} N & 0 \\ 0 & \frac{1}{N} \end{bmatrix} \begin{bmatrix} 1 & R_{SC} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_o} \\ -\overline{I_o} \end{bmatrix}, \tag{15}$$

where $$R_{SC} = \frac{(N^2+3N-2)R_{on}}{N^2(1-2\delta)}. \tag{16}$$

*Negative Converter Block:*

The equivalent circuit of the negative converter block can be analyzed in the same way. To save space, the theoretical analysis for the negative converter is omitted. The equivalent circuit of the negative converter can be obtained as follows:

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Step-up: $$\begin{bmatrix}\overline{V_i}\\ \overline{I_i}\end{bmatrix}=\begin{bmatrix}-\frac{1}{N} & 0\\ 0 & -N\end{bmatrix}\begin{bmatrix}1 & R_{SC}\\ 0 & 1\end{bmatrix}\begin{bmatrix}\overline{V_o}\\ -\overline{I_o}\end{bmatrix}, \tag{17}$$

where $$R_{SC}=\frac{(N+1)(N+2)R_{on}}{1-2\delta}. \tag{18}$$

Step-down: $$\begin{bmatrix}\overline{V_i}\\ \overline{I_i}\end{bmatrix}=\begin{bmatrix}-N & 0\\ 0 & -\frac{1}{N}\end{bmatrix}\begin{bmatrix}1 & R_{SC}\\ 0 & 1\end{bmatrix}\begin{bmatrix}\overline{V_o}\\ -\overline{I_o}\end{bmatrix}, \tag{19}$$

where $$R_{SC}=\frac{(N+1)(N+2)R_{on}}{N^2(1-2\delta)}. \tag{20}$$

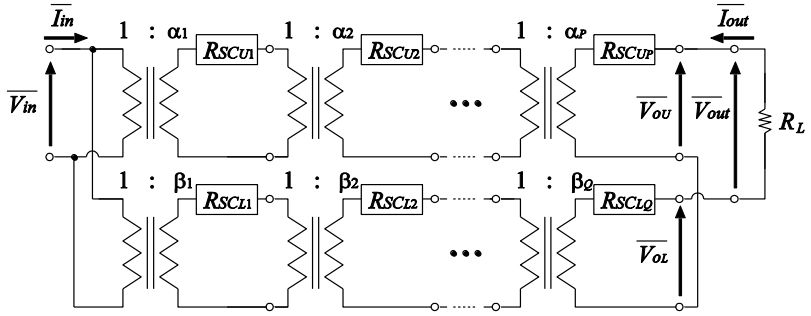


**Fig. 4:** Equivalent circuit of the proposed converter.

*Loop-Connected Converter:*

From (13) - (20), the equivalent circuit of the proposed loop-connected converter can be expressed by Figure 4. In Figure 4, $R_{scUi}$ is the SC resistance of the $i$-th upper converter block, and $R_{scLj}$ is the SC resistance of the $j$-th lower converter block. From Figure 4, we have the power efficiency and the output voltage as follows:

$$\eta_{\max}=\frac{R_L}{R_L+\sum_{i=1}^{P}\left\{\prod_{j=i+1}^{P}(\alpha_j)^2\right\}R_{scU_i}+\sum_{i=1}^{Q}\left\{\prod_{j=i+1}^{Q}(\beta_j)^2\right\}R_{scL_i}} \tag{21}$$

and $$V_{\max}=\eta\left\{\left(\prod_{k=1}^{P}\alpha_k\right)-\left(\prod_{k=1}^{Q}\beta_k\right)\right\}V_{in}, \tag{22}$$

where $$\prod_{j=i+1}^{P}(\alpha_j)^2=1 \quad (if \quad i+1>P) \quad \text{and} \quad \prod_{j=i+1}^{Q}(\beta_j)^2=1 \quad (if \quad i+1>Q).$$

*Simulation:*

Concerning the proposed converter synthesized with a positive converter block and a negative converter block, SPICE simulations are performed under conditions that $V_{in}$ = 3.7V, $R_{on}$ = 10Ω, $T$ = 100ns, $C$ = 500pF, $C_t$=$C_b$=γ$C$, and $N$=2. Figure 5 shows the simulated results of the positive converter block as a function of the output load $R_L$. In Figure 5, more than 5% of the power efficiency is improved when the output load is 10kΩ and the stray parasitic capacitance is 0.5pF. Figure 6 shows the simulated results of the negative converter block. In Figure 6, more than 8% of the power efficiency is improved by the power saving technique. Furthermore, as Figure 5 and 6 show, we can estimate the maximum power efficiency by the theoretical equations, because the theoretical result almost agrees with the SPICE simulated result when the parasitic capacitance is zero. Figure 7 shows the simulated results of the proposed loop-connected converter. Figure 7 (a) and (b) show the simulated power efficiency and the output voltage, respectively. As Figure 7 shows, the proposed converter can achieve not only a high step-up gain but also a larger number of DC-DC voltage ratios by combining positive converter blocks and negative converter blocks.

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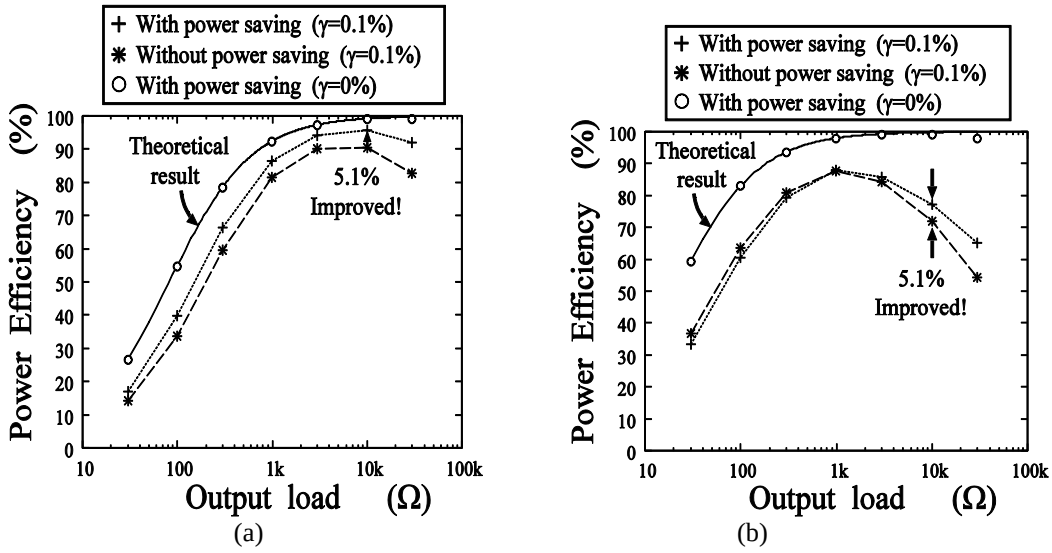


**Fig. 5:** Simulated power efficiency of the positive converter block, (a) 2 times step-up conversion and (b) 1/2 times step-down conversion.

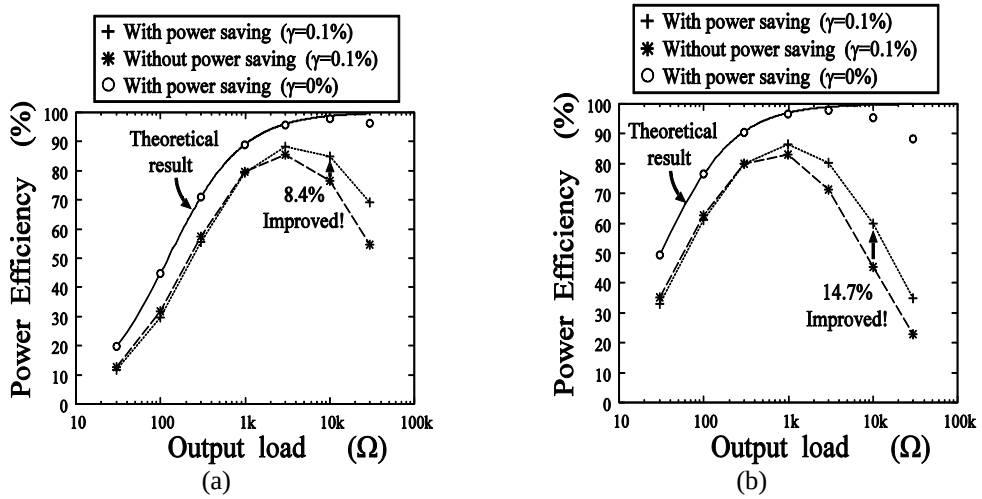


**Fig. 6:** Simulated power efficiency of the negative converter block, (a) -2 times step-up conversion and (b) -1/2 times step-down conversion.

*Experiment:*

To confirm the validity of circuit design, experiments were performed regarding to the proposed loop-connected converter synthesized with a positive converter block and a negative converter block. The experimental circuit was built with commercially available ICs AQV212 and TD62004APG on a bread board, where $V_{in}$ = 3.7V, $C_1 = C_2 = C_3 = C_4$ = 1μF, $R_L$ = 100kΩ, and $T$ = 1ms. In the experiment, we focused on the verification of the circuit topology, because the experimental circuit was built with commercially available ICs on a bread board. Figure 8 shows the measured output voltage of the converter blocks, where the 2 times and -2 times conversion are performed. In Figure 8 (a), the measured output voltage is 7.3V, where the ideal output voltage is 7.4V. On the other hand, the measured output voltage is -7.12V in Figure 8 (b), where the ideal output voltage is -7.4V. Figure 9 show the measured output voltage of the proposed loop-connected converter, where the ideal output voltage is 14.8V. From Figures 8 and 9, the validity of the proposed topology can be confirmed. The evaluation of circuit characteristics were not performed in this experiment, because the parasitic resistance of the bread board is very large unlike an IC chip. The IC implementation of the proposed converter is left to a future study.

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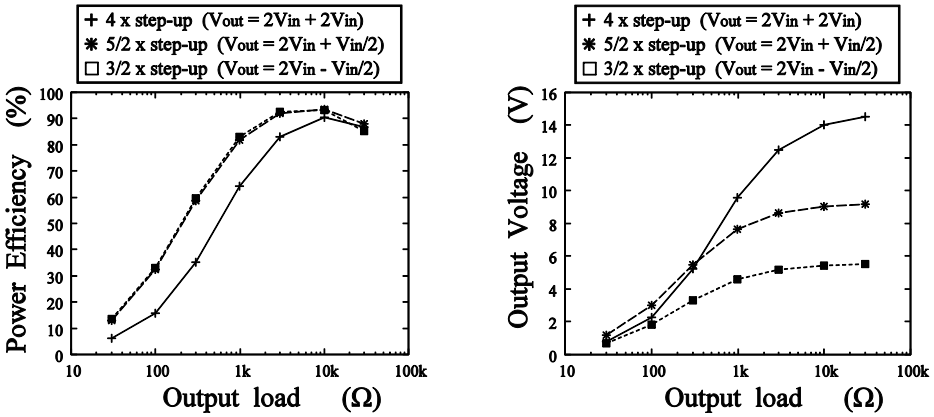


**Fig. 7:** Simulated results of the loop-connected converter, (a) Power efficiency and (b) Output voltage.

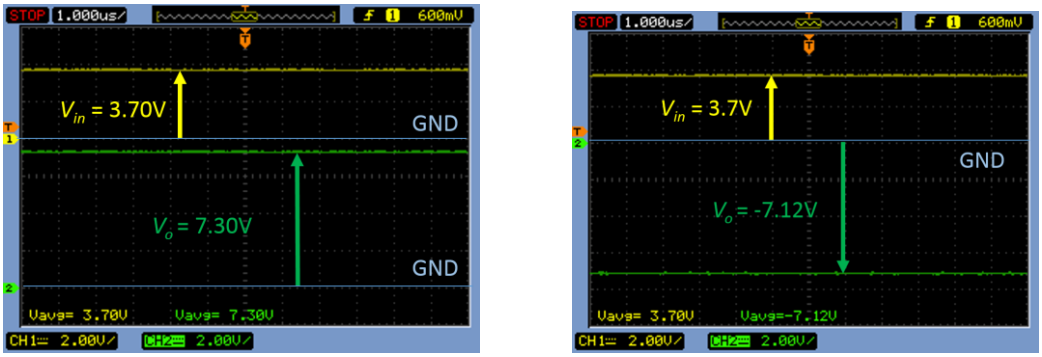


**Fig. 8:** Measured output voltage of converter blocks, (a) 2 times step-up conversion and (b) -2 times step-up Conversion.

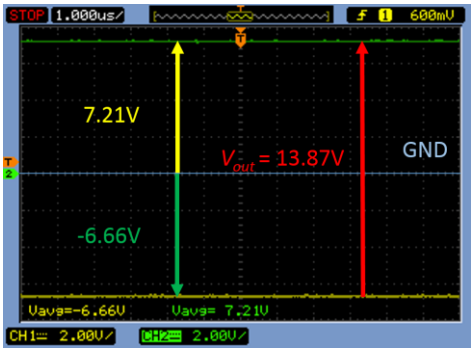


**Fig. 9:** Measured output voltage of the proposed loop-connected converter.

*Conclusion:*

To achieve a high step-up gain and flexible conversion ratios, a capacitive loop-connected topology has been proposed in this paper. The validity of the circuit design was confirmed by SPICE simulations, theoretical analysis, and experiments. To clarify the characteristics of the proposed converter, SPICE simulations, theoretical analysis, and breadboard experiments were performed.

The results of the SPICE simulations and theoretical analysis showed the following results: (1) by combining positive converter blocks and negative converter blocks, the proposed converter can achieve a larger number of DC-DC voltage ratios than the conventional series-connected converter and (2) the power saving technique can improve power efficiency effectively in the case of a small output current. Concretely, more than 5% of the power efficiency was improved in each converter block when the output load was 100kΩ and the stray parasitic capacitance was 0.5pF. Furthermore, concerning the experimental circuit built with commercially available ICs, the validity of the proposed topology was confirmed by the experiment.

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