Abnormality Detection of ECG Signals using Partial Reconfiguration in FPGA

Kalyana Sundaram C, Marichamy P, Prabha Subburam

1Assistant Professor, Mepco Schlenk Engineering College, Electronics and Communication Engineering, Sivakasi-626005, Tamilnadu, India.
2Professor, P.S.R. Engineering College, Sivakasi -626140, Tamilnadu, India.
3PG Student, Mepco Schlenk Engineering College, Electronics and Communication Engineering, Sivakasi-626005, Tamilnadu, India.

ARTICLE INFO
Article history:
Received 3 September 2014
Received in revised form 30 October 2014
Accepted 4 November 2014

Keywords:
ECG, Verilog HDL, FPGA, Vortex - 5, Partial Reconfiguration.

ABSTRACT
Reconfigurable hardware is a potential technique, which improves the performance of the systems being implemented in it. In this paper, the implementation of an ECG system for detection of abnormalities in real time has been considered using the Partial Reconfiguration technique. The implementation has been done in the Vortex-5 FPGA hardware using Verilog HDL. The performance of the implemented system has been compared with the conventional hardware. The results show that reconfiguration time of partial reconfiguration takes only 1.901 ns whereas conventional one takes 6.04 ns to detect the abnormalities in the ECG signal. The Processing Speed of the Partial Reconfiguration is three times better than the Conventional method.

INTRODUCTION

Field Programmable Gate Arrays (FPGAs) are most popularly used for reconfiguration purpose. The FPGA has the ability to reuse the same hardware for different tasks while executing an application. While the device performing the operation, we can swap the reconfiguration module. This is known as Dynamic Reconfiguration and it may produce enormous advantage in implementing a process.

Run time reconfiguration is the process of modifying a part of the device while the other portions of the device are in the running state. By using Dynamic Reconfiguration, we could potentially build a system which dynamically executes the given application within a fraction of time. This process can reduce the execution time and processing speed. By reducing the need for reconfiguration of entire device, it consumes less power and reduces energy consumption. The latest versions of FPGA provide the architectural support for Dynamic Reconfiguration. In this paper, we have designed a system which can detect the abnormalities in ECG signal using Dynamic Reconfiguration based implementation using Xilinx Vortex 5 FPGA.

While implementation, the main module is considered to have some coding that have some specific functionality. It also contains a block box based module which can also be called as non-committed modules that can be reconfigured and assembled at run-time. This module may adapt different modules that can have similar type of inputs and outputs. Instead of calling these modules separately in the program, we can instantiate a block box module and the coding can be dumped into it at the run time based on the requirement. This type of implementation may reduce the configuration time and the hardware requirement for the design implementation.

ElectroCardioGram (ECG) is a diagnostic tool that reported the electrical activity of the heart recorded by skin electrode. The morphology and heart rate indicates the cardiac health of human. Any disorder in heart rate produce changes in the morphological pattern of ECG signal and indication of cardiac arrhythmia, after measure could be detected by analyzing the waveform. Whatever the magnitude and duration of the P-QRS-T wave contains useful information about the nature of the disease that affects the heart. These electric waves are due to depolarization and polarization of heart. Sodium (Na), Potassium (K) and Calcium (Ca) deficiency can also be detected by using the ECG waveform.

The MIT-BIH arrhythmia database is used for performance evaluation of the proposed system. The MIT-BIH database contains 48 disks, each containing two channels of ECG signals for 30 min duration of 24 hours selected from the recordings of 47 individuals. The database record contains both timing information and class information.

Corresponding Author: Prabha Subburam., Electronics and Communication Engineering, Mepco Schlenk Engineering College, Sivakasi-626123, Tamilnadu, India.
Phone: 91 04562 230120; E-mail: prabhasubburam.prabha@gmail.com
MATERIALS AND METHODS

Heart arrhythmia detection has been done by using Ahlstrom and Tompkins algorithm. The coding has been written using Verilog HDL. The results have been compared with MATLAB simulated results. Certain arrhythmia can be detected by using these QRS detection algorithm (Rabiul Islam, et al., 2013).

Dynamic Partial Reconfiguration using FPGAs reduce the time for configuration and save memory as the Partial Reconfiguration files (bit streams) are smaller than full ones. Also the same fabric can be used to configure different modules based on the requirement. It shows the advantages of the newest dynamic Partial Reconfiguration design flow (Wang Lie and Wu Feng-Yan., 2009).

This paper explains about an automated Holter scanning system based on two microcomputers. QRS durations are determined using computations of first and second derivatives. Then arrhythmia analysis is done using R-R intervals and QRS durations. This system can process Holter tapes at 60 times real time and produce summaries and 24 h trend plots of several variables including heart rate and PVC count (L. Ahlstrom and Willis J. Tompkins., 1983).

The aim of this paper is to present an FPGA-oriented system design for ECG signal processing. The system performs QRS complex detection with an algorithm based on a phase-space portrait of an ECG signal, beat classification is done by a part of the Open Source ECG Analysis Software (Matej Cvikl and Andrej Zemvab., 2009).

This paper describes a Dynamic Partial Reconfiguration (DPR) design flow and Environment for Image and Signal Processing Algorithms used in Adaptive applications. A scriptable program to establish the communication between the field programmable gate array (FPGA) with IP cores and their host application, power consumption estimation of Partial Reconfiguration area and automatic generation of the partial and initial bit streams (Krill B. et al., 2010).

Modular systems implemented on Field-Programmable Gate Arrays (FPGAs) can benefit from being able to load and unload modules at run-time. Two methods for implementing Partial Reconfiguration in Virtex FPGAs are explained. One is Module based, in this type of implementation a special bus is used to communicate between modules. Only by using this bus macro, signals can pass Partial Reconfiguration boundary. Second is Difference based, here bit stream has been generated based on the difference between the two designs. Mainly used to change the LUT or memory content. In this project module based reconfiguration is used. (Sedcole P et al., 2006).

The algorithm used for the detection of T and P wave in the TP interval of the ECG signal. By using a consecutive R peak detection the slope detection of T and P wave in the TP interval of the ECG is done (Chatterjee H. K et al., 2012).

Implementation:

The ECG signal processing consists of steps like peak detection, width identification, interval variation detection. The signal to which the analysis has to be done is sampled and the discrete value has to be provided as the input to the signal. Such sampled values have been provided in the MIT-BIH database. The input has been sampled at the rate of 360 samples per second. The steps to be followed for detecting QRS complex is that follows as :

Smoothing the given input signal

\[ y_0(n) = \text{abs}[x(n+1) - x(n-1)]; \quad 2 < n < k - 1 \quad \cdots \cdots \quad (1) \]

Smoothing has been done by moving averaging filter

\[ y_1(n) = \frac{y_0(n-1) + y_0(n) + y_0(n+1)}{4}; \quad 2 < n < k - 1 \quad \cdots \cdots \quad (2) \]

Rectified second order derivative

\[ y_2(n) = \text{abs}[x(n+2) - 2x(n) + x(n-2)]; \quad 3 < n < k - 2 \quad \cdots \cdots \quad (3) \]

\[ y_3(n) = y_1(n) + y_2(n); \quad 3 < n < k - 2 \quad \cdots \cdots \quad (4) \]

Then the primary threshold can be determined as

Primary threshold \( = 0.8 \text{ma} x[y_3(n)]; \quad 3 < n < k - 2 \quad \cdots \cdots \quad (5) \)

Secondary threshold \( = 0.1 \text{ma} x[y_3(n)]; \quad 3 < n < k - 2 \quad \cdots \cdots \quad (6) \)

From the above equations the primary and secondary threshold value has been set. The R peak has been detected by considering that, the actual sample should have threshold above the primary threshold value and the next 5 samples should have the threshold above secondary threshold value.
The R peak has been detected by applying the above equations. The RR interval has been determined by using the formula

If the sampling frequency is Fs Hz. Then time for one sample is given as

\[ T_s = \frac{1}{F_s} \text{ second} \quad \ldots \ldots \quad (7) \]

If R-R interval is N samples then,

\[ R - R \text{ Interval in time} = T_s \times N \text{ second} \quad \ldots \ldots \quad (8) \]

By using above eight equations, we can detect R peak and the R-R interval. Now by considering the relative positions of R-R peak we can detect the location of P and T peak. As the sampling frequency are 360 samples per second. Let us consider the R peak sample value as S. And for the normal signal the P and T peak can be located at the positions between S-60 and S+60 respectively. By locating the peak and by providing the window of width 40 by placing the peak at the center, we can determine the width of the P and T wave.

Fig. 1: Basic shapes in ECG signal

Fig 1 shows the actual width and amplitude of ECG signals. For the abnormal signals the width may vary (i.e.) it may widen or narrow down and it can be determined by varying the window size. The amplitude variation in abnormal signal shows the variation in electrical activity of heart. Also the relative locations of peak may vary depending on the number of R peaks at the given interval (i.e.) the width may reduce with increase in the number of beats per minute. By adjusting the window size, we can locate the P and T peaks. By using these values we can determine the type of Arrhythmia, Magnesium, Potassium and Calcium imbalance and Thyroid deficiency (hypothyroidism) can also be determined by using the location of amplitude and width of the peaks in ECG signal.

Architectural Implementation:

Fig. 2: Block diagram of algorithm implementation

Fig 2 shows the implementation steps to be followed in detecting the abnormality in ECG signal. While implementing using Partial Reconfiguration, the derivative and threshold detection steps are coded in main module. The peak, width and amplitude detection steps are written as reconfigurable module which can be implemented as a single block box and the coding has been loaded during the runtime based on the requirement which reduces amount of hardware require for configuring the given algorithm. Instead of implementing all the four modules we can write one main module and one reconfigurable module and instant loading can be done.
Results:

Implementation of the proposed algorithm utilized resources of FPGA in the manner shown in the table1. The resource utilized by direct implementation is more than Partial Reconfiguration implementation. Run time reconfiguration has been used in this method. Based on the requirement partial bit stream has been loaded.

Table 1: Comparison of device utilization using Partial Reconfiguration and direct implementation

<table>
<thead>
<tr>
<th>Logic utilization</th>
<th>Available</th>
<th>Used without PR</th>
<th>Used with PR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slice Registers</td>
<td>86400</td>
<td>249</td>
<td>74</td>
</tr>
<tr>
<td>Number of LUT’s</td>
<td>86400</td>
<td>318</td>
<td>108</td>
</tr>
<tr>
<td>Global clock buffer</td>
<td>32</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>I/O BUFFERS</td>
<td>480</td>
<td>78</td>
<td>21</td>
</tr>
</tbody>
</table>

The schematic diagram for the design implementation of both direct and Partial Reconfiguration has been shown as in the Fig 3 and 4.

Fig 3: Schematic diagram with Partial Reconfiguration

Fig 4: Schematic diagram without Partial Reconfiguration

Fig 5 shows the simulation result produced at each step. Width, amplitude and peak width of the P, QRS and T wave at each time period is also shown. Simulation result of the above implementation is given as

Fig 5: Simulation result of algorithm implementation
The peak and width detection of QRS, P and T waves has been done. The number of beats per second is also being determined by measuring the number of R peaks at the interval of one minute. By using these measurements we can determine the abnormality in the given input signal. Table 2 shows some of the abnormalities that can be detected by using the above procedure.

Table 2: Abnormalities detected using above given algorithm

<table>
<thead>
<tr>
<th>Abnormal Component</th>
<th>Actual Range</th>
<th>Description</th>
<th>Possible Causes</th>
</tr>
</thead>
<tbody>
<tr>
<td>P waves</td>
<td>0.12 sec</td>
<td>Absent</td>
<td>Atrial fibrillation, sinus node arrest, Hyperkalemia</td>
</tr>
<tr>
<td>T wave</td>
<td>0.5 to 0.9 mV</td>
<td>Tall</td>
<td>Hyperkalemia, Left Bundle Branch Block, Stroke, Ventricular Hypertrophy</td>
</tr>
<tr>
<td>T wave</td>
<td>0.5 to 0.9 mV</td>
<td>Small, flattened, or inverted</td>
<td>Myocardial Ischemia, Electrolyte Disturbances, Pulmonary Embolism, Conduction Disturbances, Hypokalemia</td>
</tr>
<tr>
<td>PR interval</td>
<td>0.12 to 0.2 sec</td>
<td>Long</td>
<td>First-degree Atrioventricular block.</td>
</tr>
<tr>
<td>PR interval</td>
<td>0.12 to 0.2 sec</td>
<td>Varying</td>
<td>Type I Atrioventricular block, Multifocal Atrial Tachycardia</td>
</tr>
<tr>
<td>QRS complex</td>
<td>0.06 to 0.12 sec</td>
<td>Wide</td>
<td>Right or Left Bundle Branch Block, Ventricular flutter or Fibrillation, Hyperkalemia</td>
</tr>
<tr>
<td>QT interval</td>
<td>0.4 sec</td>
<td>Long</td>
<td>Myocarditis, Hypocalcaemia, Hypomagnesaemia, Hypokalemia, Hypothyroidism, Stroke.</td>
</tr>
<tr>
<td>QT interval</td>
<td>0.4 sec</td>
<td>Short</td>
<td>Hypocalcaemia, Hypermagnesemia</td>
</tr>
<tr>
<td>P-P interval</td>
<td>0.66 to 1 sec</td>
<td>Varying</td>
<td>Sinus Arrhythmia</td>
</tr>
</tbody>
</table>

By comparing Table 2 and by the measurements we obtain from above algorithm implementation, we can detect the abnormalities and the chemical imbalance in the human body.

Table 3 shows no of peaks detected by the algorithm implemented and the actual peak found in the input waveform. The input given as 10 second samples taken from the MIT-BIH arrhythmia database.

Table 3: Number of Peaks detected by the algorithm

<table>
<thead>
<tr>
<th>Sample No</th>
<th>No of R peak present</th>
<th>No of R peak detected</th>
<th>Sensitivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>101</td>
<td>10</td>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>103</td>
<td>10</td>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>116</td>
<td>14</td>
<td>13</td>
<td>92.85</td>
</tr>
<tr>
<td>122</td>
<td>15</td>
<td>14</td>
<td>93.33</td>
</tr>
<tr>
<td>123</td>
<td>8</td>
<td>8</td>
<td>100</td>
</tr>
<tr>
<td>208</td>
<td>9</td>
<td>9</td>
<td>100</td>
</tr>
<tr>
<td>214</td>
<td>15</td>
<td>14</td>
<td>93.67</td>
</tr>
<tr>
<td>116</td>
<td>14</td>
<td>13</td>
<td>92.85</td>
</tr>
</tbody>
</table>

The sensitivity of the algorithm is above 90% and this shows the effectiveness of the algorithm being used.

Conclusion:

Implementation of one of the effective algorithm using FPGA hardware with Partial Reconfiguration improves the Performance and Operation speed. The minimum period of implementation is 1.901 ns for partial reconfiguration. Implementation without Partial Reconfiguration takes 6.04 ns of minimum period implementation. The implementing speed can also be made better by using some parallel implementation. Computational Speed of the algorithm with Partial Reconfiguration is three times better than the Conventional Method, which implies it decreases the power consumption of the device.

REFERENCES

Chatterjee, H.K et al., 2012. Real time P and T wave detection from ECG using FPGA. Procedia Technology, pp: 840-844.


Krill, B et al., 2010. An efficient FPGA-based dynamic Partial Reconfiguration design flow and


Sheikh Md. Rabiul Islam et al., 2013. FPGA based Heart Arrhythmia’s Detection Algorithm. ACEEE Int. J. on Information Technology, 1(3).
