STBC-OFDM Downlink Baseband Receiver

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ABSTRACT

This project presents the adaptive frequency domain channel estimation in multiple input multiple-output (MIMO) orthogonal frequency-division multiplexing (OFDM) modems with high bit rate. The combination of MIMO transmission, OFDM technology, comprises a promising solution for next-generation wireless communications. Here we can choose VLSI platform for implementation because of hardware complexity. MIMO technology has attracted attention in wireless communications, because it offers significant increases in data throughput and link range without additional bandwidth or transmit power. In OFDM a large number of closely-spaced orthogonal sub-carriers are used to carry data. The data is divided into several parallel data streams or channels, one for each sub-carrier. Each sub-carrier is modulated with a conventional modulation scheme (such as Quadrature amplitude modulation or phase-shift keying) at a low symbol rate, maintaining total data rates similar to conventional single-carrier modulation schemes in the same bandwidth.

INTRODUCTION

A modem (modulator-demodulator) is a device that modulates an analog carrier signal to encode digital information, and also demodulates such a carrier signal to decode the transmitted information. The goal is to produce a signal that can be transmitted easily and decoded to reproduce the original digital data. Modems can be used over any means of transmitting analog signals, from driven diodes to radio. Multiple inputs multiple outputs OFDM system provides reliable communication with bandwidth efficiency and high throughput rate. In radio, multiple-input and multiple-output, or MIMO (commonly pronounced my-moh or me-moh), is the use of multiple antennas at both the transmitter and receiver to improve communication performance. It is one of several forms of smart antenna technology. MIMO technology has attracted attention in wireless communications, because it offers significant increases in data throughput and link range without additional bandwidth or transmit power. It achieves this by higher spectral efficiency (more bits per second per hertz of bandwidth) and link reliability or diversity (reduced fading). Because of these properties, MIMO is a current theme of international wireless research.

Table I: Major Parameters of The Proposed Stbc-Ofdm System

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF frequency</td>
<td>2.5 GHz</td>
</tr>
<tr>
<td>System channel bandwidth (BW)</td>
<td>10 MHz</td>
</tr>
<tr>
<td>Sampling frequency (Fs)</td>
<td>11.2 MHz</td>
</tr>
<tr>
<td>Sampling factor</td>
<td>28/25</td>
</tr>
<tr>
<td>FFT size (N)</td>
<td>1024</td>
</tr>
<tr>
<td>Subcarrier spacing (Δf)</td>
<td>10.9 kHz</td>
</tr>
<tr>
<td>Useful symbol time (T_s)</td>
<td>91.4 μs</td>
</tr>
<tr>
<td>Guard time (T_g)</td>
<td>11.4 μs</td>
</tr>
<tr>
<td>OFDM symbol duration (T_d)</td>
<td>102.9 μs</td>
</tr>
<tr>
<td>Number of OFDM data symbols in a DL sub-frame</td>
<td>40</td>
</tr>
<tr>
<td>DL</td>
<td>Number of pilot subcarriers (N_pilot)</td>
</tr>
<tr>
<td>PUSC</td>
<td>Number of data subcarriers (N_data)</td>
</tr>
</tbody>
</table>

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In this paper, an STBC-OFDM downlink baseband receiver for mobile WMAN is proposed and implemented. First, a novel match filter is proposed to precisely detect symbol boundary. Moreover, a ping-pong algorithm is presented to improve the performance of carrier frequency synchronization. Then, we propose a two-stage channel estimator to accurately estimate CSI over fast fading channels (Ku and Huang, 2008). The initialization stage uses discrete Fourier transform (DFT)-based channel estimation with the multipath interference cancellation (MPIC)-based de-correlation to identify significant channel paths (Lin et al., 2008).

The tracking stage uses decision-feedback (DF) DFT-based channel estimation with Newton’s method to track the gain variations of these paths (Alamouti, 1998). The proposed baseband receiver designed in 90-nm CMOS technology can support up to 27.32 Mbps down-link (uncoded) data transmission under 10 MHz channel band-width. This design has a core area of 24×24 lm² and dissipates 68.48 mW at 78.4 MHz operating frequency. This paper includes the following features:

- provision of a STBC-OFDM downlink baseband receiver architecture that is capable of high-speed transmission at high mobility;
- integration of a simple and robust synchronizer and an accurate but hardware affordable channel estimator to overcome the challenge of outdoor fast fading channel;
- implementation of a successful STBC-OFDM downlink baseband receiver for mobile WMAN.

**Fig. 1:** Proposed STBC-OFDM system with two transmit antennas and one receive antenna.

**System architecture:**

The proposed STBC-OFDM system is based on IEEE 802.16e OFDMA specification and supports the distributed subcarrier allocation of partial usage (PUSC) for downlink (DL) transmission. The major parameters are summarized in Table I. The fast Fourier transform (FFT) size N is set to 1024. The length of cyclic prefix (CP) is 128 sampling periods. The modulation schemes of quadrature phase shift keying (QPSK) and 16quadrature amplitude modulation (16QAM) are supported for data subcarriers, while binary phase shift keying (BPSK) is adopted for pilot subcarriers and preamble symbols. A DL sub-frame is composed of one preamble symbol and 40 OFDM data symbols. The system design target is to support carry frequency offset (CFO) up to ±14 ppm and is optimized to enable the vehicle speed up to 120 km/hr. The maximum Doppler frequency fD is about 0.025 (normalized to a subcarrier spacing). The coherence time T calculated by a typical way is 1.5 ms which is about 14.8 times of an OFDM symbol time but is smaller than a frame time. Therefore, the channel can be treated as quasi-static within several symbol times but may vary a lot during one frame transmission (Alamouti, 1998).

Fig. 1 shows the proposed STBC-OFDM systems with two transmit antennas and one receive antenna. In the transmitter, serial data first pass through the constellation mapper and then pass through serial-to-parallel (S/P) to form two transmitted symbols during a time slot which is equivalent to two OFDM symbol times. These two transmitted symbols are encoded by Alamouti’s STBC scheme (Deneire et al., 2003), transformed by \( N \)-point inverse fast Fourier transform (IFFT), and inserted with a guard interval \( T \) to prevent inter-symbol interference (ISI). A complete OFDM symbol with the symbol duration is transferred to an analog signal by a digital-to-analog (D/A) converter, filtered by a low-pass filter (LPF), up converted to RF band, and transmitted. The signal is received from an antenna, down converted to the baseband, low-pass filtered, and digitized by an analog-to-digital (A/D) converter. The proposed baseband receiver consists mainly of two parts: synchronizer and channel estimator. The channels are assumed to be quasi-static within any two successive OFDM symbol durations. Hence, without loss of generality, the received signal processing is focused on each time slot, which is two OFDM symbol times, and the time index of symbol transmission is omitted hereafter except other-wise mentioned.
Proposed baseband receiver design:

Fig. 2 shows the architecture of the proposed downlink baseband receiver. The proposed receiver includes a symbol boundary detector, an integer carrier frequency offset (ICFO) estimator, a fractional carrier frequency offset (FCFO) estimator, an FFT, a two-stage channel estimator, an STBC decoder, and a de-mapper.

A. Simple and Robust Synchronization:
Synchronization includes symbol timing, sample clock, and carrier frequency synchronization. The proposed synchronizer concentrates on the symbol boundary detection and the carrier frequency recovery loop as presented in the following sections.

1) Symbol Boundary Detection: An ISI free region of symbol timing detection is determined by the difference in length between the CP and the channel impulse response (Deneire et al., 2003). Since the proposed system has two transmit antennas, the signals transmitted from different antennas may arrive at the receiver with different delays due to multipath effect. Therefore, the decided boundary must locate in the common ISI free region to prevent the respective ISI effects from other symbols. IEEE 802.16e standard provides three types of preamble subcarrier sets which can be expressed as

\[ \text{PreambleCarrierSet}_k = s + 3 \cdot k \]

Where \( s = 0, 1, \) and \( 2 \) is the subcarrier set index, and \( k \) denotes a running subcarrier index.

However, the mismatch of oscillator frequency in a receiver and a transmitter causes frequency offset effects in the received signals and destroys the characteristic of the matching results. In order to overcome this problem, we propose a modified match filter. The filter coefficient sequence which is the known preamble sequence is compensated with the possible values of ICFO. An output peak will appear in matching with the preamble sequence compensated with the corresponding ICFO. Hence, this match filter has an additional advantage that the coarse ICFO can be detected simultaneously.

2) Carrier Frequency Recovery: After symbol boundary has been successfully obtained, the CP position is known. The CP repeating characteristic can be used to estimate FCFO by correlating the CP with the corresponding received sample sequence. However, when the CFO value is in the middle of two integer values, the accuracy of ICFO detection by using the match filter method is substantially decreased. Because the ICFO effects caused by these two integer values are almost the same, there are two indistinguishable peaks in the matching results. The indistinguishable peaks caused by noise and another antenna interference may easily result in wrong ICFO detection. Therefore, a ping-pong algorithm is proposed to improve the performance of ICFO detection. The ping-pong algorithm partitions each CFO region into the strong region and the weak region depending on the distance to each integer value, as shown in Fig. 3. The accurately estimated FCFO value can be used to correct the ICFO detection. When the estimated FCFO value locates in the strong region, the matching results have strong reliability to determine ICFO by detecting the peak value. When the estimated FCFO value locates in the weak region, there are two possible peaks in the matching results. Thus, the ICFO value will be adjusted by the information of the FCFO value and these two peaks.

If the ICFO value is detected to be 1 directly depending on the output peak, the estimated CFO is 1.4. This result is unreasonable because another peak is 0 but not 2. By using this ping-pong algorithm, the ICFO value will be correctly adjusted to be 0.

Fig. 3: CFO region partition for the proposed ping-pong algorithm.
B. Accurate Two-Stage Channel Estimation:

Two major categories of pilot-aided channel estimation methods are interpolation-based channel estimation methods and DFT-based channel estimation methods (Deneire et al., 2003). Interpolation-based method estimates channel frequency response (CFR) by interpolating the received pilot subcarriers. This method is not suitable for outdoor fast fading channels. This is because the channel coherent bandwidth becomes small, and using the interpolation-based method with limited pilot information becomes more difficult to recover channel variations. DFT-based method focuses on transform domain to characterize time-domain channel impulse response (CIR) and effectively improves the performance by suppressing time-do-main noise. Many DFT-based methods derived from maximum likelihood (ML) scheme have been studied for OFDM systems with preambles. In order to further improve the estimation performance, the DF DFT-based channel estimation method is employed by using decided data subcarriers as pilot subcarriers to track channel variations for saving transmission bandwidth and providing sufficient tracking information.

A two-stage channel estimation method is used to realize a successful STBC-OFDM system in outdoor mobile channels. The multipath fading channel is characterized by CIR consisting of a few significant paths. The delays of these paths usually vary slowly in time, but the path gains may vary relatively fast. Therefore, in the initialization stage, the significant paths are identified during the preamble symbol time. In the tracking stage, the path gain variations in the identified path positions will be tracked in the following data symbol transmission. Fig. 4 shows the architecture of the two-stage channel estimator.

1) Initialization Stage: The operation blocks in this stage are a preamble match, an IFFT, a straight multipath interference cancellation (SMPIC)-based decorrelator, and an FFT. The pre-amble match correlates the received signal with the frequency-domain preamble symbol to get the preliminary CFRs of different antenna pairs. Then, the CIR $\tau_{\text{Preamble}}[\cdot]$ can be obtained.

2) Tracking Stage: The operation blocks in this stage are an STBC decoder, a data de-mapper, a least-square (LS) estimator, an IFFT, a Hessian matrix calculator, a path decorrelator, and a FFT. To have the fine local optimization capability for estimating time-varying channels, the DF DFT-based channel estimation method combining with Newton’s method is adopted.

Table II: Word Lengths Of Several Key Signals In The Proposed Receiver.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Word Length</th>
<th>Signal</th>
<th>Word Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Received Sample Input</td>
<td>10</td>
<td>Preamble Match Output</td>
<td>12</td>
</tr>
<tr>
<td>CORDIC Input</td>
<td>14</td>
<td>LS Estimator Output</td>
<td>14</td>
</tr>
<tr>
<td>CORDIC Output</td>
<td>14</td>
<td>STBC Decoder Output</td>
<td>9</td>
</tr>
<tr>
<td>FFT Output</td>
<td>13</td>
<td>IFFT/FFT Output</td>
<td>16</td>
</tr>
<tr>
<td>FFT Twiddle Factor</td>
<td>18</td>
<td>SMPIC Decorrelator Output</td>
<td>14</td>
</tr>
<tr>
<td>Channel Response Output</td>
<td>16</td>
<td>Path Decorrelator Output</td>
<td>14</td>
</tr>
</tbody>
</table>

We take the hardware implementation and performance issues into the consideration in the algorithm and system development. The proposed baseband receiver design has the following features.

• The proposed match filter applied with the ICFO-compensated coefficients can reduce the CFO effect and provide the precise symbol boundary detection, and the ICFO value can be detected simultaneously.

• The proposed ping-pong algorithm using the estimated FCFO value can refine the ICFO value and improve the accuracy.

• The proposed two-stage channel estimation can highly improve the performance in outdoor mobile channels as compared with the interpolation-based methods that are frequently adopted in the baseband implementation.

• In the initialization stage, the proposed SMPIC-based decorrelator uses a straightforward method to identify significant paths and cancel the multipath interference, which can highly reduce the implementation cost.

• In the tracking stage, the matrix inverse computation is efficiently avoided by employing the strongly diagonal property, which can highly save the computation complexity.

Architecture and circuit design:

The decision of signal word lengths affects the system performance and hardware complexity. The output SNR at the STBC decoder is used as a performance criterion to determine the appropriate word lengths of each building block. The word lengths of several key signals in the proposed receiver are summarized in Table II.

A. Synchronizer:

In the match filter, each tap performs complex multiplication of the coefficient and the received sample. If the coefficients are quantized into the tap operation can be simplified to add or subtract the received sample.
avoids the multiplier usage and reduces the register requirement. However, the sign calculation is necessary due to subtraction, and more hardware effort is required for sign extension. Therefore, if the signed calculation is avoided, the hardware and power will be further saved. In the proposed method, both the real and imaginary parts of the received sample are quantized. The quantization loss is less than 0.8 dB in SNR, and it can be compensated by increasing the matching length $L$, which costs only a little hardware overhead.

According to the simulation results at the vehicle speed of 120 km/hr, the matching length of 300 is chosen in this case so that the symbol miss error probability approaches the lowest boundary. The match filter design is shown in Fig. 5. A monitor circuit is used to count $N_M$ after each data updating. The tap results are generated by the logical circuits and are accumulated to obtain $N_1$ by a carry save adder (CSA) tree. A logical circuit can be simplified to use only NAND gate and NOR gates. In the proposed symbol boundary detection, the coefficient sequence is pre-shifted with the possible values of ICFO, so that the ICFO can be detected simultaneously. The coefficient sequence is stored in ROM. In order to accumulate the matching results twice for ICFO detection, an additional circuit is necessary to store the previous matching results as shown in Fig. 6. If the control signal is positive, the registers will respectively store the current matching results of the possible ICFO values. On the contrary, if a control signal is negative, the chain of the registers works as the shift-registers for accumulating the matching results. Finally, the accumulated results are passed to the comparator to select the two ICFO values that have maximum peaks in the accumulated results.

Fig. 5 shows the cross correlation circuit for the FCFO estimation, and the FCFO estimate is derived from the phase of this complex correlation output. In FCFO estimation, a 1024 delay-line is necessary to store the received data and to do the correlation. Shift registers for realizing the delay-line will cost a lot of area and power consumptions.

![Fig. 5: Block diagram of the proposed match filter.](image)

![Fig. 6: Storage units for storing the previous matching results.](image)

### B. Two-Stage Channel Estimator:

The operation of the proposed channel estimator (see Fig. 4) contains the initialization stage and the tracking stage. The FFT/IFFT module can be shared between these two stages.

1) **Initialization Stage:** The preamble match is used to estimate preliminary CFRs. The preamble subcarrier values are boosted as a constant power. To avoid the multiplier usage in matching calculation, the absolute value of the normalized preamble subcarrier can be expressed as a constant canonical signed digit (CSD) code. The preamble match design only requires adders and multiplexers controlled by the sign of the preamble patterns. Thus, only the sign bits of the preamble patterns are stored. The SMPIC-based decorrelator is used to identify the significant paths in a straightforward method. In this design, $N_C$ is 128 and is same as the CP length, and $N_M$ is presumed to be eight. Based on the output SNR evaluation at the vehicle speed of 120 km/hr, the $N_M$ value is decided to be four. The SMPIC-based decorrelator consists of a partial sorting network and a decorrelator. An 8-item sorter arranged with eight memory modules are used for partial sorting. The sorter is based on the Batcher’s sorting network, and the basic unit is a 2x2 comparator which is used to perform data comparison and exchange. The memory modules are used to store the path power values. The merge sorting procedure is used two times to sort the 128 to 32-item data and the 32 to 8-item data (Park et al., 2006).

2) **Tracking Stage:** By using dividers, the STBC decoder can be implemented intuitively. However, a divider is very costly. The FFT and IFFT are required by the proposed two-stage channel estimator and can be shared by the initialization stage and the tracking stage. A parallel memory-based FFT/IFFT architecture with multiple
inputs and outputs in normal order is used to have a lower cost and reduce the latency which is targeted to be less than 1/4 of an OFDM symbol time. 1024-point FFT/IFFT module that is composed of eight independent memory modules, four radix-8 processing elements (PEs), two radix-2 butterfly elements, and two commutators. The memory modules are implemented with single-port SRAM modules which consume less area and power than dual-port SRAM modules.

C. Data Flow:
In the proposed baseband receiver, the time-domain OFDM symbols after phase compensation are passed through the FFT processor for OFDM demodulation. The frequency-domain OFDM symbols are then passed to the channel estimation and STBC decoding modules. Since the STBC-OFDM system has two transmit antennas and one receive antenna, two received OFDM symbols in a time slot must be ready at the same time for channel estimation and STBC decoding. Thus, the FFT processor along with five memory banks, MB_R1_0, MB_R1_1, MB_R1_2, MB_R2_0, and MB_R2_1, are used to perform OFDM demodulation and buffer the received OFDM symbols. After phase compensation, a time-domain OFDM symbol is written into one of these five memory banks for FFT processing. While FFT processing, the time-domain received OFDM symbol is continuously written to another memory bank.

Conclusion:
In this paper, we proposed a downlink baseband receiver for mobile WMAN that is applied in the STBC-OFDM system with two transmit antennas and one receive antenna. A simple symbol boundary detector, a carrier frequency recovery loop modified by the ping-pong algorithm, and an accurate two-stage channel estimator are effectively implemented. Although the two-stage channel estimator requires higher hardware cost as compared with the interpolation-based channel estimators, it has significant performance improvement for successfully environments.

REFERENCES


