Low Voltage Schmitt Trigger In 0.18 µm CMOS Technology

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ABSTRACT

Schmitt Trigger circuit is widely used in analogue and digital circuit to solve the noise problem. Hysteresis is a common drawback of the Schmitt Triggers which is determined by the device dimensions, process parameters and supply voltages. This study presents a Schmitt Trigger circuit which can operate at low voltage. The proposed circuit is designed based on Conventional Schmitt Trigger by manipulating the arrangement of transistors’ width-length ratio. The design is carried out in 0.18 µm CMOS technology using Mentor Graphics. From the simulation results, it is found that the proposed design can operate as low as 0.8V. The circuit offers less propagation delay compared to the conventional circuit. It can be widely used in various low voltage analogue and digital applications.

Key words: CMOS, Capacitance, Hysteresis Schmitt Trigger, Transistor

Introduction

The Schmitt trigger, introduced by Otto Schmitt in 1930s (Schmitt, 1938), has been commonly used in the field of communication and signal processing techniques for improving on/off control, reducing the noise effects in triggering devices, analogue to digital conversion (Mohd-Yasin et al., 2004; Reaz et al., 2007; Marufuzzaman et al., 2010; Chavez, 1995; Akter et al., 2008) and a number of other emerging applications including frequency doublers, retinal focal-plane sensors, sub-threshold SRAM, image sensors, pulse width modulation circuits, wireless transponders, FPGA based system and sensors etc. (Dejhan et al., 2004; Reaz et al., 2006; Reaz and Wei 2004; Mogaki et al., 2007; Yuan, 2009; Reaz et al., 2003; Romli et al., 2012; Reaz et al., 2005; Singhanath et al., 2011). A common drawback of Schmitt triggers is the hysteresis determined by the device dimensions, process parameters and supply voltages(Kuang, and Chuang, 2001). As a result, the hysteresis varies with process conditions and a spread of the parameters has to be tolerated from chip to chip as well as from batch to batch.

Several approaches have been proposed to implement Schmitt trigger(Kader et al., 2012). A conventional Schmitt trigger is shown in Fig. 1. A detailed design was proposed by Filanovsky and Baltes (1994) where the switching thresholds are dependent on the ratio of NMOS and PMOS. However, the design exhibited racing phenomena when the transition started. A low voltage Schmitt trigger is proposed in this paper which can operate from 0.8V-1.5V at high capacitance with less propagation delay and stable hysteresis width by lowering the supply voltage (Kulkarni and Roy, 2012; Lotze and Manoli, 2012).

Materials And Methods

The proposed design is a combination of two sub-circuit, P Sub-Circuit (which consists of P1, P2 and P3) and N sub-circuit (which consists of N1, N2 and N3) as in Fig. 2.
There is no direct connection between the source voltage and ground as P sub-circuit is connected to the path between the source voltage and output while the N sub-circuit is connected between the path of output and
ground. Therefore, there is no static power consumption as there is no direct path between source voltage and ground.

Part 1 of the proposed circuit forms a NAND gate and designed according to De Morgan’s Theorem. Two PMOS (P1 and P2) are formed by a parallel connection while two NMOS (N1 and N2) are formed by a series connection. By designing the PMOS in parallel, the resistance of the P sub-circuit will be reduced by halves. Thus, the propagation delay can be reduced as shown in Equation 1:

$$t_p = 0.69RC_l = \frac{t_{phl} + t_{plh}}{2}$$

(1)

The PMOS delay is reduced because delay is more concentrated to PMOS due to high mobility of PMOS compared to NMOS. Part 2 of the proposed schmitt trigger consists of a PMOS, (P3) and a NMOS, (N3) where both the MOSFET is directly connected through the gate terminal of each. The P3 act as pull up while the N3 act as a pull down for the output at each case.

The sizes of the transistors are set by locating the minimum component path of each sub-circuit. Each of the transistors is sized according to their arrangement. The transistors in series are scaled by factor of 2 each while transistors in parallel are scaled by a factor of 1 each. The PMOS and NMOS ratio is set according to Equation 2 with the effective length, $L_{eff} = 0.18 \text{ m}$ (for 0.18 technologies).

$$\left(\frac{W}{L_{eff}}\right)_{\text{PMOS}} = r \left(\frac{W}{L_{eff}}\right)_{\text{NMOS}}$$

(2)

The PMOS transistor is widen so that the resistance matches the pull down NMOS device. Typically, $r = 3 \rightarrow 3.5$ (Sapawi et al., 2008). Therefore, the ratio is set to 3 to maximize the noise margin and to create a circuit with symmetrical Voltage-Transfer Characteristic (VTC). By increasing the width of PMOS, it moves the switching threshold voltage towards VDD, which makes the hysteresis width more rectangles as desired by a Schmitt trigger design.

When the input is low, only the P sub-circuit will be considered and causes the output to be high (equal to VDD). During this condition, both P1 and P2 are on, but P3 is off (because $V_{SG} < |V_{tp}|$ as P3’s source voltage and gate voltage is equal). Therefore, the output voltage is pulled to VDD. When the input increases to VDD, N1 and N2 is turned on. Thus, the output voltage is pull down to ground. Mentor Graphic has been used to for designing the proposed Schmitt Trigger. The schmetic diagram is shown in Fig. 3.

**Results And Discussions**

The Three designs are simulated using Mentor Graphic software. The 1st design represents the conventional Schmitt TRIGGER with the transistor ratio proposed by (Wang et al., 1997). The 2nd design represents the design where the transistor ratio is kept as per this proposed design. The 3rd design is the proposed Schmitt trigger. The respective transistor dimensions for the three designs are shown in Table 1. The comparison is made in term of propagation delay.

**Table 1: The Transistor Dimension**

<table>
<thead>
<tr>
<th>$\frac{W}{L_{eff}}$</th>
<th>1st Design</th>
<th>2nd Design</th>
<th>3rd Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>1.44</td>
<td>1.08</td>
<td>0.54</td>
</tr>
<tr>
<td></td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>P2</td>
<td>1.44</td>
<td>1.08</td>
<td>0.54</td>
</tr>
<tr>
<td></td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>P3</td>
<td>0.18</td>
<td>0.54</td>
<td>0.54</td>
</tr>
<tr>
<td></td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>N1</td>
<td>1.8</td>
<td>0.36</td>
<td>0.36</td>
</tr>
<tr>
<td></td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>N2</td>
<td>1.8</td>
<td>0.36</td>
<td>0.36</td>
</tr>
<tr>
<td></td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>N3</td>
<td>1.44</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td></td>
<td>0.18</td>
<td>0.18</td>
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</tr>
</tbody>
</table>
The proposed design is tested at 0.8, 1.0, 1.2 and 1.5V. The compilation of the simulation result is shown in Fig. 4.

![Compilation of simulation results at various voltages](image)

**Fig. 4:** Compilation of simulation results at various voltages

The result as shown in Fig. 4 shows that the proposed Schmitt Trigger can be successfully operated and can be used in low source voltage operation condition. The propagation delays are less in high voltage source compared to low voltage due to the transistor effective resistance and wire.

![Comparison of propagation delay](image)

**Fig. 5:** Comparison of propagation delay

The comparison of the propagation delay between the designs is showed in Fig. 5. These results show that the proposed design is the best design in low source voltage in terms of propagation delay. The layout design is shown in Fig. 6.

![Layout design](image)
Conclusion:

A new CMOS Schmitt trigger is presented in this study. The proposed design is capable to function at as low as 0.8 voltage. The circuit offers less propagation delay compared to the conventional circuit. It can be widely used in various low voltage analogue and digital applications.

References


